Analogue WFEE with a 130 nm BiCMOS process

Two quasi-identical **Low-Noise Amplifiers** (one with the possibility of input offset compensation) fully differential, ultra-low 1/f noise frequency, low-gain drift and high linearity
+ a **Current Reference** with four outputs of 2.2 mA, low drift
+ two **slow Digital-to-Analogue Converter** of 8-bit (one of [0, 2.2 mA], the other of [0, 600 μA]), with a pair of differential outputs, ultra-low 1/f noise frequency, low INL and low drift
+ an **On-Chip Thermometer**
+ Components to be characterised.

FEATURES

Differential voltage LNA

- **Voltage gain**
  - Bare gain: 164 V/V
  - Loaded gain: 82 V/V
  - Loaded gain, including input matching: 41 V/V
- **Input noise**
  - Intrinsic equivalent input noise $e_n < 0.7$ nV/$\sqrt{\text{Hz}}$; $i_n < 3$ pA/$\sqrt{\text{Hz}}$
  - Total input noise spectral density with 200 Ω source $\sqrt{S_v} < 1$ nV/$\sqrt{\text{Hz}}$ @ f>50 Hz
  - Total input noise spectral density with 200 Ω source and using R_{FB} for input-matching $\sqrt{S_v} < 0.5$ nV/$\sqrt{\text{Hz}}$ @ f>50 Hz
- **1/f noise frequency** ≈ 10 Hz
- **Current noise** 2-3 pA/$\sqrt{\text{Hz}}$
- **Gain drift** <250 ppm/K
- **Bandwidth** DC-15.7 MHz (-1 dB)
- **PSRR** ≈ 79 dB ±2% Vcc @ 9 MHz
- **CMRR** > 85 dB @ 9 MHz
- **Output dynamic range** up to 1 V_{pp}
- **3.3 V voltage supply** (V_{cc}=+1.65 V, V_{ee}=-1.65 V, V_{cm}=0 V)
- **Differential input impedance** 8 kΩ
- **Differential output impedance** 6 Ω

Current Reference

- **4 outputs** of 2.2 mA
- **Temperature compensation** with I_{CTAT} and I_{PTAT}
- **3.3 V voltage supply** (Vcc = +1.65 V, Vee = -1.65 V)

slow D/A Converters

- **8 bits**
- **FSR** one with 2.2 mA max. and the other with 600 μA max.
- **Resolution** 8.6 μA @ Imax = 2.2 mA; 2.4 μA @ Imax = 600 μA
- **Voltage compliance** 1 V
- **3.3 V voltage supply** (Vcc = +1.65 V, Vee = -1.65 V)

Thermometer

- **Temperature range** from 10 °C to 80 °C
- **Thermometer sensitivity** up to hundreds of mV/K
- **Output signal** up to 2.7 V_{pp}. Output differential current drives output resistors connected to any common-mode voltage in between 1.65 V and −1.65 V (usually 0 V). Maximum dynamic range observed with 1.36 V common-mode voltage (*ie* middle between Vcc and Vee).
- **3.3 V voltage supply** (Vcc = +1.65 V, Vee = -1.65 V)

GENERAL DESCRIPTION

AwaXe_v4 (*Athena Warm Asic for the X-ifu Electronics - version 4*) is an upgrade ASIC developed for the Warm Front End Electronics (WFEE) of the X-IFU (X-ray Integral Field Unit) instrument in the context of the future X-ray space telescope ATHENA. It belongs to the AwaXe and SQmux ASIC families developed at APC for the SQUID/TES readout. Within the series, this is the first version based on the ST 130 nm SiGe BiCMOS process.

As shown in Figure 1, this ASIC integrates two differential Low-Noise Amplifiers (LNAs) , two 8-bit slow Digital-to-Analogue Converters (slowDACs) with different output ranges, a current reference (Iref) with identical four outputs, a thermometer for temperature housekeeping, two identical PNP current mirrors that accept strong bias current up to 10 mA and elementary components such as bipolar transistors (npnvhv, pnpl), MOSFETs(nmos25, pmos25), a capacitor (CMIM) and a resistor (Rpolysab). However, it does not integrate the digital component of the WFEE, a series bus RS485/I^{2}C to configure the slow DACs, which will be included in the next ASIC.

SPECIFICATIONS

Power supply = 3.3 V for all analogue devices: V_{cc} = +1.65 V, V_{ee} = −1.65 V, V_{cm} = 0 V (1.65 V above V_{ee}).

For the 8 bits that configure the output current of the two slowDACs, use -1.65 V as the low level (0) and 0.35 V (or 0.85 V max) as the high level (1).

Nominal operating temperature = 300 K, unless otherwise noted. Tested operating temperature range: 0 °C to 80 °C

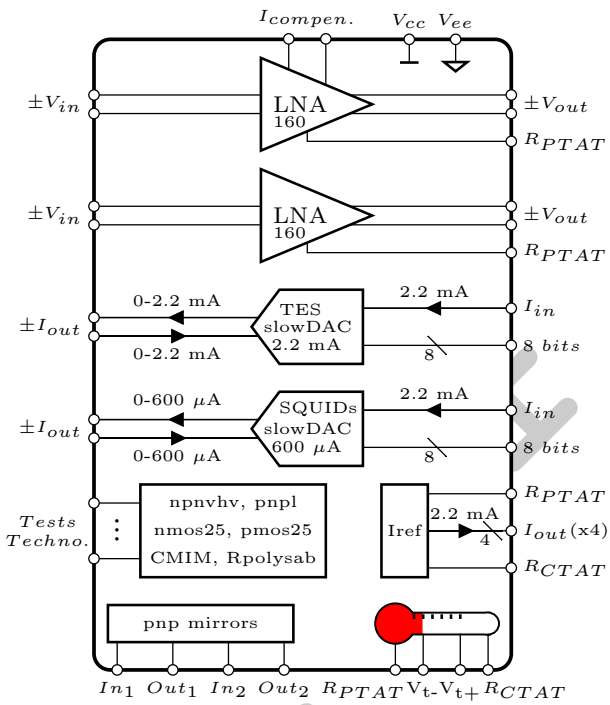

Figure 1: Block diagram of the AwaXe_v4 including all analog devices of the WFEE.

LNA

BLOCK DIAGRAM

The LNA is a fully differential amplifier, with 2 inputs and 2 outputs (Figure 2). It equips independent bias current reference proportional to temperature (PTAT) with a reference resistor R_{PTAT} to generate the bias current (Typical simulated value R_{PTAT} = 340 Ω). The current through R_{PTAT} should be about 170 μA to provide correct bias and normal functionalities. A bias current too small will degrade linearity yet too large will cause a smaller gain. Due to process gradient, the required R_{PTAT}'s value may vary from ASIC to ASIC. Before applying LNA, users should first check the bias current by measuring the voltage at the edge of R_{PTAT} (about 58 mV with 340 Ω). With this level of bias current, the LNA will consume around 45 mA, which could be another

index to check LNA's operating status.

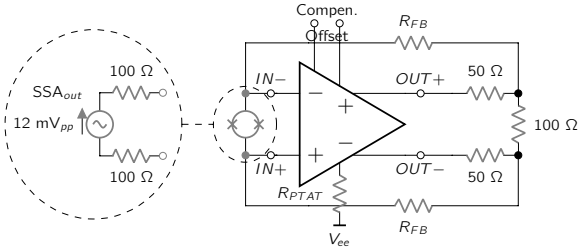

Figure 2: Simplified schematic of the LNA with external resistors basic connections. R_{PTAT} = 470 Ω was used for the characterisation.

The output impedance matching can be achieved by connecting two resistors at the differential output. The differential intrinsic output impedance is about 6 Ω, much smaller than the load of 100 Ω. Figure 2 illustrates a typical example with two 50 Ω at the outputs to adapt a resistive load of 100 Ω.

The intrinsic input impedance is basically the ratio $\frac{\beta}{g_m}$. The simulation showed about 8 kΩ differential input impedance. In the case of input impedance matching, a feedback resistor R_{FB} can be used to connect OUT+ and IN− and another one to connect OUT− and IN+. This input matching is based on the Miller effect. Hence, the value of R_{FB} depends on the source's differential resistance R_S and the gain inside the feedback loop: $R_{FB} = \frac{R_S}{2} \times (\text{Gain} + 1)$. At the output side, the feedback can be connected either directly to the output terminals, or the load as shown in Figure 2. For the former case, the gain is the intrinsic gain of the LNA, about 160 V/V. For the latter case, the gain is half because of the output matching, thus about 80 V/V. For example, if R_S = 200 Ω, $R_{FB} = \frac{200}{2} \times (\frac{160}{2} + 1)$ = 8100 Ω.

TYPICAL PERFORMANCE

The simulations of the amplifier have generally considered parasitic components introduced by input and output pads by connecting a capacitor of 3 pF to V_{SS} and an inductor of 10 nH at each input and output. The LNA uses a PTAT resistor of 340 Ω to provide a bias current. The voltage across R_{PTAT} should be about 57.8 mV, so that the current $I_{PTAT} \approx 170$ µA. The feedback resistors R_{FB} of 8350 Ω are used to match the differential source impedance of 200 Ω.

Table 1: LNA performance

	Typ	Unit
Gain, DC-10 MHz		
Intrinsic	164	V/V
Loaded	82	V/V
Loaded, with input matching	41	V/V
Bandwidth of the gain of 80		
-1 dB	15.7	MHz
-3 dB	30.4	MHz
Equivalent input noise		
white	<1	nV/$\sqrt{\text{Hz}}$
1/f @1 Hz	1.46	nV/$\sqrt{\text{Hz}}$
Other parameters		
Phase @10 MHz	20	°
1/f Corner Frequency	10	Hz
Non-linearity on 1 $V_{diff-out_{pp}}$	<1	%
Gain drift [17°C, 37 °C]	<250	ppm/K
PSRR, DC-1 MHz	>90	dB
CMRR, DC-1 MHz	> 100	dB
Max input offset correction	10	mV
Consumption	150	mW

Differential Voltage Gain and Phase

Simulated gain is shown on the top of Figure 3. The intrinsic gain is about 160 V/V. With a load of 100 Ω and two 50 Ω in series at the output, the loaded gain is about 80 V/V, with a division of 2. Further considering input matching that introduces another factor of 0.5, the gain becomes about 40 V/V.

The bandwidth of loaded gain (≈80 V/V) is about 15.72 MHz with -1 dB compression and 30.42 MHz with -3 dB compression. Output at the load has a phase shift of about 22° at 10 MHz comparing to the input of the LNA[1], as shown in Figure 3 on the bottom.

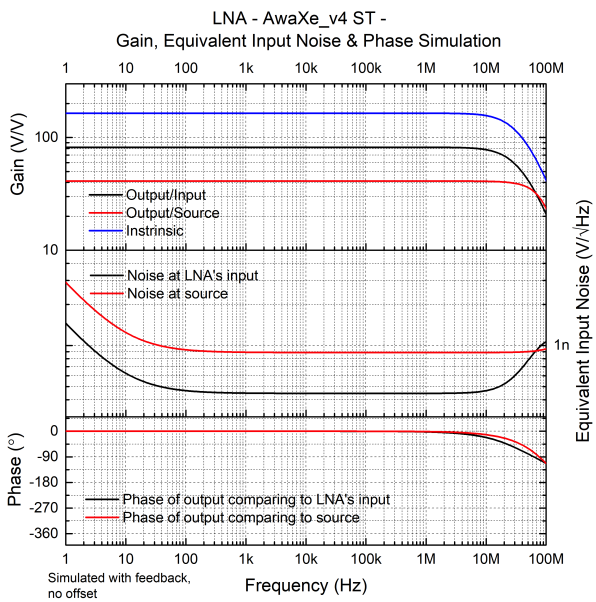

Figure 3: Simulated gain (top), equivalent input noise (middle) and phase (bottom), loaded, input matching taken into account (red curves) or not (black curves)

Equivalent Input Noise

The noise of the amplifier illustrated in the middle of Figure 3 is characterised by input voltage e_n and current noises i_n. The total input voltage noise density $\sqrt{S_v}$ is the contribution of both input noise, where the current noise contribution is via the differential impedance of the source R_S. The main noise contributors include the input and output shot noise of the front-end bipolar transistors, thermal voltage noise from the parasitic access resistance of the base of the front-end bipolar transistors, the noises generated by the second stage of the LNA and thermal noise of the two feedback resistors R_{FB}.

Thanks to the input matching, the equivalent noise at the input of the LNA is half of the equivalent noise at the source. Yet, the signal-noise ratio keeps the same. The white noise at the source is lower than 1 nV/$\sqrt{\text{Hz}}$@ f > 50 Hz. 1/f noise at 1 Hz at source is about 2.9 nV/$\sqrt{\text{Hz}}$ and 1.46 nV/$\sqrt{\text{Hz}}$ at the input of the LNA with 1/f corner frequency close to 10 Hz.

Offset Compensation

An offset of about 10 mV will be constantly at the input of the LNA during operation, due to the source impedance and cable resistance with SQUIDs bias current passing through. 10 mV offset indeed requires a dynamic range of at least 20 mV_{pp} that surpasses the specification of this LNA of 12 mV_{pp}. Hence, an offset compensation has been integrated into one of the two LNAs in the ASIC "AwaXe_v4".

The LNA with the compensation option has two pads "Offset1_LNA_OS" and "Offset2_LNA_OS", to connect to an external current source. The compensation current indeed generates an opposite offset to compensate the offset due to bias current. Figure 4 shows noise and gain evolution corresponding to different offset levels, created either by bias and compensation current or only by compensation current. It needs about 1.42 mA to compensate 10 mV offset, which leaves output offset close to 0, instead of 0.8 V without any compensation. It allows the LNA to operate normally (Figure 4). The equivalent input noise of the LNA increases with a higher current to

[1] The phase measurement does not concern the LNA's own stability, but could be useful if the LNA is used in a feedback loop for considering the loop's stability.

compensate larger offset. The loaded gain stays almost the same since the offset is well compensated. Moreover, the manufacturing influence has also been verified with Monte-Carlo simulations, as shown in Figure 5.

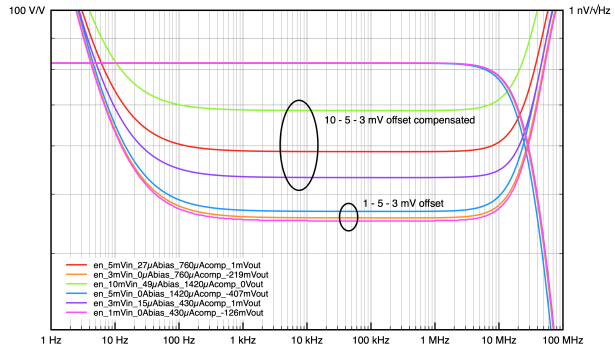

Figure 4: Gain and equivalent input noise simulations with different levels of input offset, bias current and compensation current. Simulated with the LNA, two slow DACs and the current reference integrated into the ASIC "AwaXe_v4". The bias current is generated by a slow DAC of 600 µA and the compensation current by a slow DAC of 2 mA.

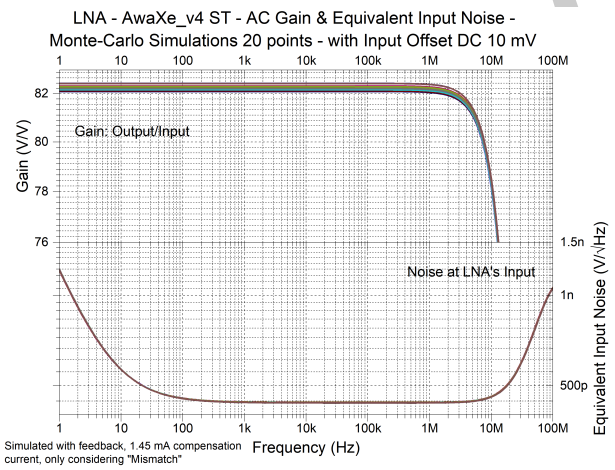

Figure 5: Gain of 80 V/V and equivalent input noise at the input of LNA - Monte-Carlo 20 points simulations with offset 10 mV at input and 1.45 mA compensation current. Only considering "mismatch".

Input Impedance

The intrinsic input impedance of the LNA is indeed very high, close to 1 MΩ, thanks to the instrumentation amplifier topology, as shown in Figure 6 (black line on the top). Although it starts to decrease before 1 MHz due to parasitic capacitors, the input impedance is still higher than 30 kΩ at 20 MHz. With two 8350 Ω feedback resistors for the input matching, the input impedance (the red line on the top) is stable at 200 Ω up to 10 MHz.

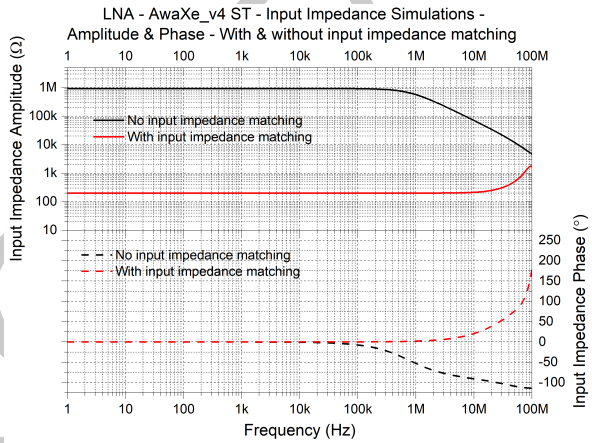

Figure 6: Simulated LNA input impedance with or without the resistive feedback for the input impedance matching. (Top) Amplitude of the impedance; (Bottom) Phase of the impedance.

Stability

Step response to a large dynamic square wave (V_{in}=12 $mV_{pp-diff}$ and V_{out} ≈ 0.5 $V_{pp-diff}$) with 1 ns rising and falling edge shows good stability (Figure 7). The simulation has taken into account both input matching and load, with the gain of 40 V/V that is the worst case to test stability. A capacitor of 3 pF and an inductor of 10 nH were connected to each input and output representing parasitic components.

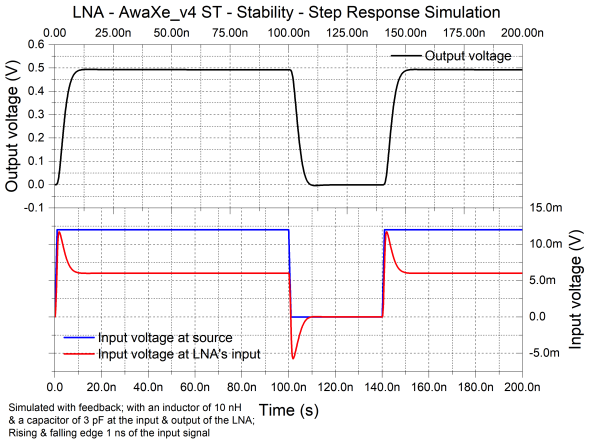

Figure 7: Simulated LNA output response (black curve on the top) to 12 mV_{pp} square signal from source (blue curve on the bottom). The red curve on the bottom is the signal at the input of the LNA.

Linearity

Quasi-static response show non-linearity lower than 1% up to 18 mVpp input signal (Figure 8). The LNA has been optimised to have 1% non-linearity (THD: Total Harmonic Distortion) at 9 MHz with the loaded gain of about 80 V/V. It allows using a smaller bias current for the output stage to reduce consumption. Lower frequency has milder distortion: the THD at 1 MHz is about 0.16%.

Gain drift

The LNA of "AwaXe_v4" uses a current reference PTAT for bias, namely the current is proportional to temperature. It allows mitigating the variation of transconductance g_m to produce a stable gain. Figure 9 illustrates the gain drift of the LNA between 17 °C and 37 °C, smaller than 250 ppm/K within this range. The top curves are the drift of the gain of 80 V/V and the bottom ones are of 40 V/V. The large signal gain (pss) of 80 V/V was simulated without feedback because this is a worse situation.

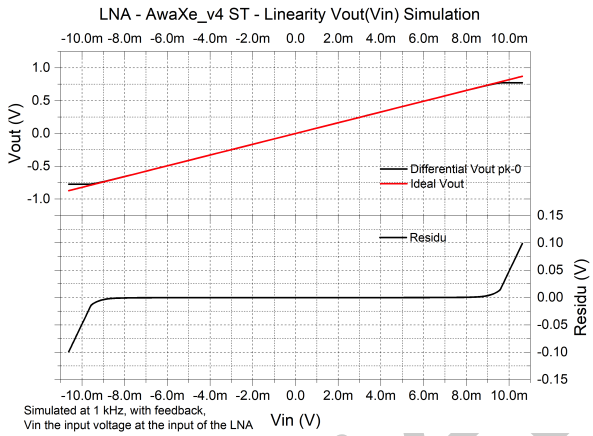

Figure 8: (top) Quasi-DC (simulated at 1 kHz) Vout as the function of Vin amplitude (black curve) and ideal Vout with gain of 84.6 V/V (red line); (bottom) Residual corresponds to the ideal gain. The Vin and Vout are peak-to-0 values that need to be doubled when referred to peak-to-peak requirements. Saturation is clearly visible at Vin > 9.5 mV_{pk-0} namely 19 mV_{pp} and Vout > 0.75 V_{pk-0}, namely 1.5 V_{pk-0}.

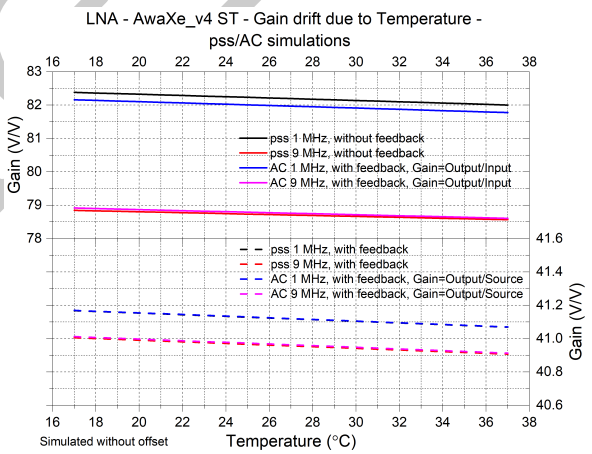

Figure 9: Gain drift versus temperature variation: (top) Gain of about 80 V/V; (bottom) Gain of about 40 V/V

CMRR

Monte-Carlo simulations are used to verify the common mode gain of the LNA (Figures 10 and 11).

The CMRR (Common-Mode Rejection Ratio) at 1 MHz and 9 MHz can be de-

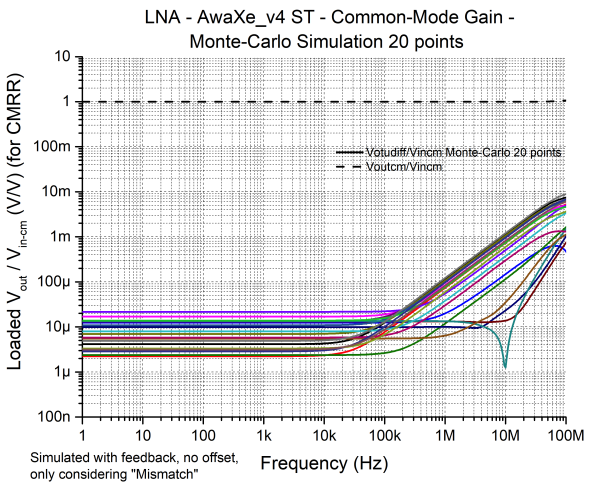

Figure 10: Common-mode gain responding to a common-mode input of 1 V AC signal common-mode rejection of the LNA: Differential-mode output/Common-mode input (20 solid lines from Monte-Carlo simulations); Common-mode output/Common-mode input (dashed line).

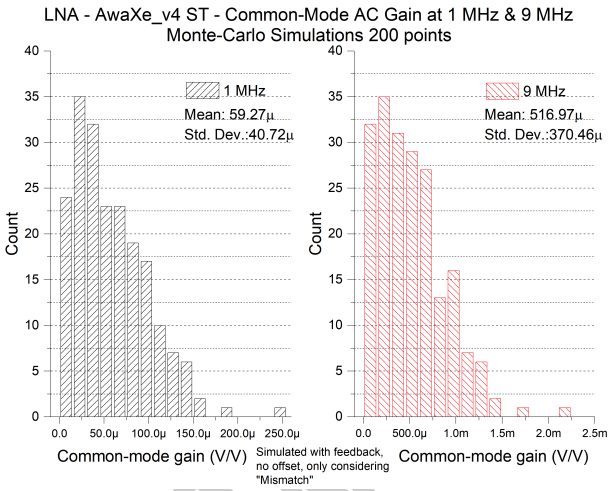

Figure 11: Monte-Carlo simulations of 200 points for the common-mode gain distribution at 1 MHz and 9 MHz.

duced from the simulations shown in Figure 11 with eq. 1.

$$\mathrm{CMRR(dB)} = 20\log_{10}\left(\frac{A_d}{A_c}\right) \qquad (1)$$

With A_d ≈41.12 V/V and A_c ≈150 µV/V (worst case), CMRR at 1 MHz≈108.76 dB.

With A_d ≈40.96 V/V and A_c ≈1.5 mV/V (worst case), CMRR at 9 MHz≈88.72 dB.

PSRR

Figure 12 shows the simulation gain with different levels of power supply, representing the static power supply rejection. Evidently, there is a degradation when lowering the power supply more than 0.25 V from 3.3 V. Indeed, simulations showed that the variation of 3.3 V power supply must be kept below 2% to keep a good PSRR (Power Supply Rejection Ratio). PSRR can be calculated with eq. 2.

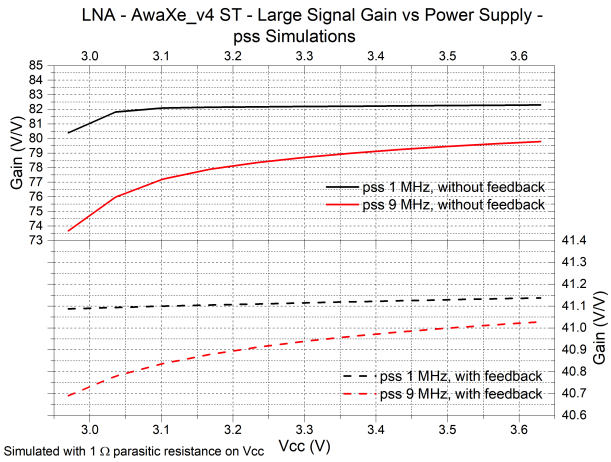

Figure 12: Loaded large signal gain without (top) or with (bottom) input matching vs power supply.

$$\begin{aligned}\mathrm{PSRR(dB)} &= 20\log_{10}\left(\frac{\Delta V_{\text{power supply}}}{\Delta V_{out}} \times \mathrm{Gain}\right)\\ &= 20\log_{10}\left(\frac{\Delta V_{\text{power supply}}}{\frac{V_{out}}{\mathrm{Gain}} \times \Delta\mathrm{Gain}} \times \mathrm{Gain}\right)\end{aligned} \qquad (2)$$

With input matching and within 2% variation of power supply, the large signal gain's drift is about 120 ppm/2% V_{cc} at 1 MHz, corresponding to PSRR≈93.17 dB. At 9 MHz, the drift is about 607 ppm/2% V_{cc}, corresponding to PSRR≈78.99 dB.

Another simulation by applying a 1 V AC signal at power supply verifies the power supply rejection in terms of AC, as shown in Figure 13. Using eq. 2, the PSRR according to the Monte-Carlo simulations of the differential output varies between 120-150 dB at low frequencies.

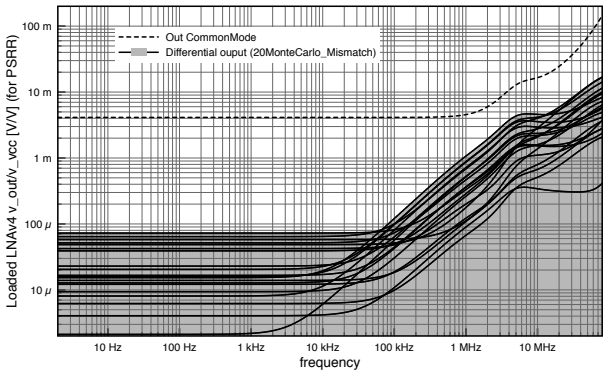

Figure 13: Voltage output of common mode (dashed line) and of differential mode (solid lines from Monte-Carlo simulations) responding to a 1 V AC signal at power supply to show the power supply rejection of the LNA.

Current reference

BLOCK DIAGRAM

This device is destined to generate reference current for slow DACs of the WFEE. This version has 4 identical outputs of about 2.2 mA (I_{ref1-4}). It combines a Proportional-To-Absolute-Temperature (PTAT) reference and a Complementary-To-Absolute-Temperature (CTAT) reference for acquiring a stable current independent of temperature. So, two resistors, R_{PTAT} and R_{CTAT}, need to be connected outside the ASIC, as shown in Figure 14.

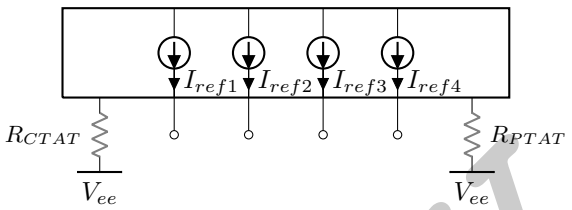

Figure 14: Simplified schematic of the current reference with basic external connections of resistors. R_{CTAT} = 2700 Ω and R_{PTAT} = 420 Ω were used for simulations.

The recommended combination of the resistors is R_{CTAT} = 2700 Ω and R_{PTAT} = 420 Ω. It is optimised for the slow DACs, to output low-drift current around MSB level close to 300 K, when all 4 outputs are connected. If less than 4 outputs are used, the optimised value could be different. Moreover, the process gradient may cause a drift of the optimum region where thermal fluctuation is the best compensated. In such a case, it is suggested to adjust the R_{PTAT} and R_{CTAT} to have a better performance. Furthermore, the output current level can also be adjusted by using different resistance.

TYPICAL PERFORMANCE

The current reference in the ASIC "AwaXe_v4" is an independent component that can be used either alone or with slow DACs via connections on PCB. It has 4 identical outputs connected to PNP bipolar transistors of the current mirrors inside. Because the PNP BJT has rather limited current gain $\beta \approx 80$, yet each branch outputs about 2.2 mA, changing the numbers of output connected will cause an important variation of base current. Consequently, the optimised value of R_{CTAT} and R_{PTAT} are different. The simulations shown in this section were done with all 4 outputs connected. Table 2 resume the simulated performance.

Table 2: Current reference performance

	Typ	Unit
Output current	2.2	mAdc
Consumption[2]	34	mW
Drift		
Optimised for Iref	[-22.7, 40.9]	ppm/K
Optimised for DAC MSB	[83.8, 145.8]	ppm/K
Output current noise		
white, before filtering	100	pA/$\sqrt{Hz}$
white, after filtering	0.4	pA/$\sqrt{Hz}$
1/f @1 Hz, before filtering	170	pA/$\sqrt{Hz}$
1/f @1 Hz, before filtering	151	pA/$\sqrt{Hz}$
Corner frequency		
before filtering	2	Hz
after filtering	<500	Hz

Output current drift

If operating independently, R_{CTAT} = 2.7 kΩ and R_{PTAT} = 460 Ω are proposed to optimise the output drift between 17°C and 37°C, as shown in Figure 15. The drift

[2] With all four outputs of 2.2 mA connected. There is about 1 mA over consomption resulting from leaking currents at the ground pin of lateral PNP bipolar transistors.

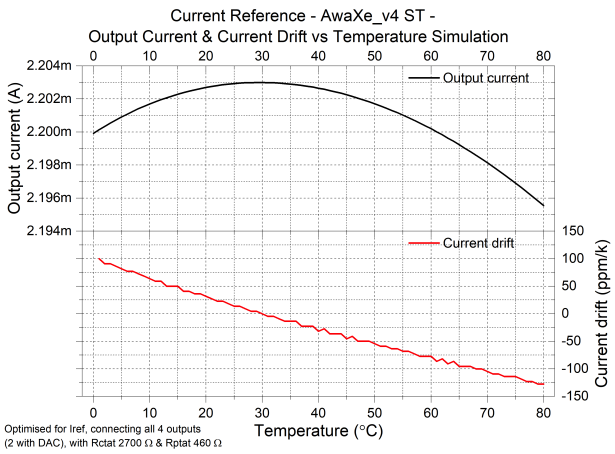

Figure 15: (top) Output current vs temperature; (bottom) Current drift vs temperature. With R_{CTAT} = 2.7 kΩ and R_{PTAT} = 460 Ω, optimised for current reference within [17°C, 37°C]

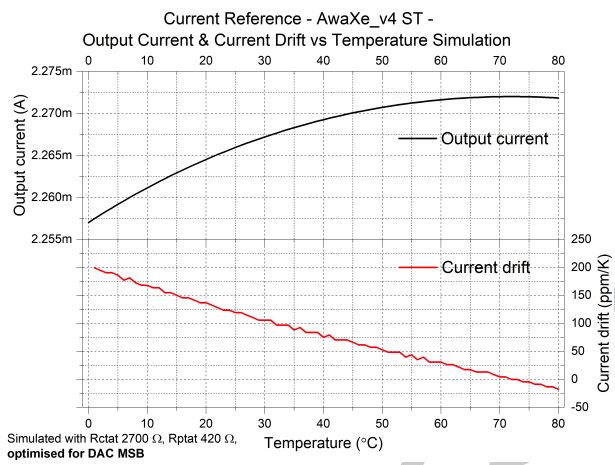

Figure 16: (top) Output current vs temperature; (bottom) Current drift vs temperature. With R_{CTAT} = 2.7 kΩ and R_{PTAT} = 420 Ω, optimised for slow DACs within [17°C, 37°C]

equals about 40.9 ppm/K at 17°C, about -22.7 ppm/K at 37°C and close to 0 around 27°C (300 K).

If operating with slow DACs, R_{CTAT} = 2.7 kΩ and R_{PTAT} = 420 Ω are proposed to optimise the output drift of DAC at MSB level between 17°C and 37°C. Then, the drift of the reference's output is no longer optimised, as shown in Figure 16. The drift equals about 145.8 ppm/K at 17°C and 83.8 ppm/K at 37°C.

Output current noise

Figure 17 shows the simulation of output current noise with or without connecting a capacitor of 100 µF and a resistor of 825 Ω at the output for filtering. These two components are to be mounted on PCB, to filter the noise between the reference and slow DACs.

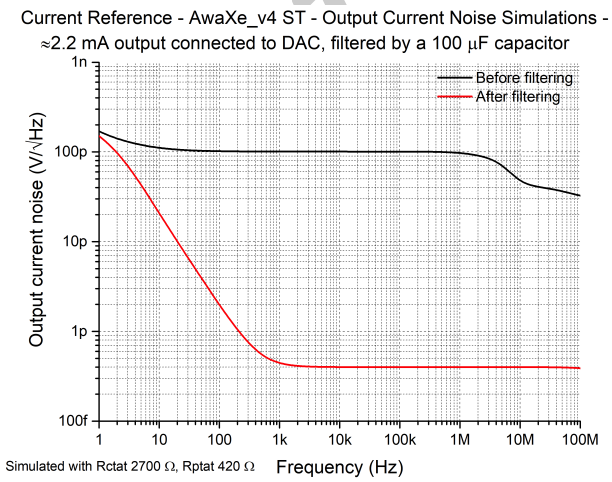

Figure 17: Output current noise simulations with (red curve) or without (black curve) connecting a capacitor of 100 µF and a resistor of 825 Ω at the output o the reference for filtering.

slow DACs

BLOCK DIAGRAM

The ASIC integrates 2 slow DACs with different output ranges: [0, 600 µA] and [0, 2.2 mA], represented by the diagram in Figure 18. Each DAC has a positive output (I_{source}) and a negative output (I_{sink}), quantised by their proper 8 bits (b_0-b_7) into 256 levels. They require a current input of about 2.2 mA to operate correctly, thus should be connected to one of the outputs of the current reference on PCB.

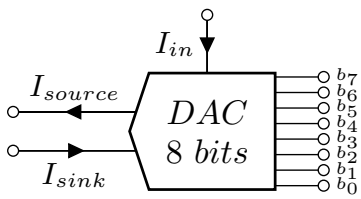

Figure 18: Simplified schematic of the slow DACs.

TYPICAL PERFORMANCE

Current slow DACs

Tables 3 and 4 resume the simulated performances of slow DACs of 2.2 mA and 600 µA. The simulations always applied the current reference integrated into the ASIC to bias the DACs.

Table 3: 2.2 mA Slow DAC performance

	Typ	Unit
Output current	2.2	mAdc
INL	< 3.5	LSB
Drift of MSB, [17°C, 37°C]	< 55	ppm/K
Output impedance @20 MHz	1800	Ω
Consumption[3]	20.1	mW
Output current noise		
white	[3, 52.7]	pA/√Hz
1/f @1 Hz	[9.3, 1100]	pA/√Hz

[3]Here only considers the DAC's own consumption without taking into account the input current of 2.2 mA consuming by the current reference.

Table 4: 600 µA Slow DAC performance

	Typ	Unit
Output current	600	µAdc
INL	< 3.3	LSB
Drift of MSB, [17°C, 37°C]	< 106	ppm/K
Output impedance @20 MHz	3200	Ω
Consumption[4]	10.1	mW
Output current noise		
white	[1, 18.2]	pA/√Hz
1/f @1 Hz	[2.8, 296]	pA/√Hz

Output & INL (Integral Non-Linearity)

Figure 19 shows the differential output and INL (residual) of the DAC of 2.2 mA, and Figure 20 of 600 µA. The two DACs have similar INL performance about 3 LSB.

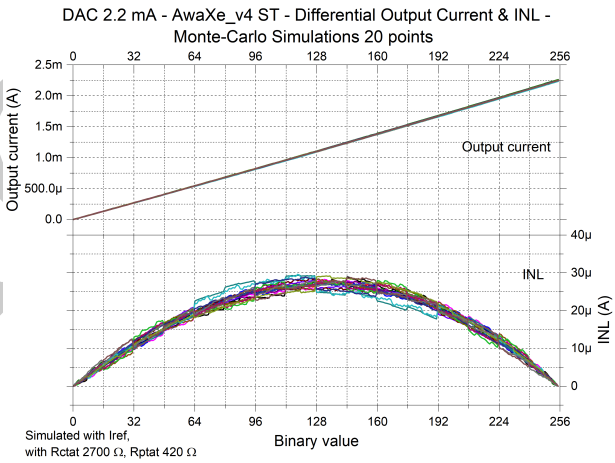

Figure 19: Monte-Carlo simulation of the 2.2 mA DAC showing differential output (Top) and Residuals (Bottom) of 256 levels. 1 LSB is about 8.6 µA.

Output current noise

Figures 21 and 22 show the simulated output current noise of 2.2 mA and 600 µA DACs, both with 9 levels of output: from

[4]Here only considers the DAC's own consumption without taking into account the input current of 2.2 mA consuming by the current reference.

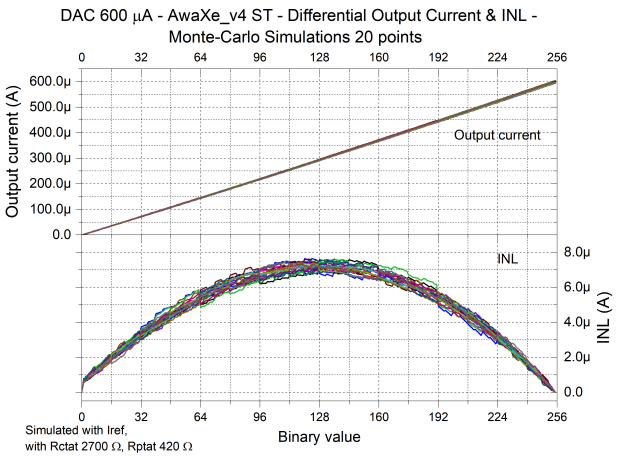

Figure 20: Monte-Carlo simulation of the 600 µA DAC showing differential output (Top) and Residuals (Bottom) of 256 levels. 1 LSB is about 2.4 µA.

LSB up to the maximum current. A capacitor of 100 µF along with an 825 Ω resistor is connected between the output of the current reference and the input of each DAC for the simulation to filter the reference output noise down to 2 Hz.

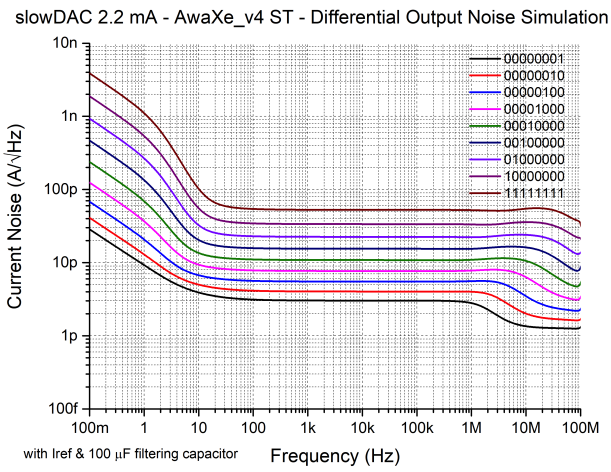

Figure 21: Output current noise of 2.2 mA DAC, with 9 levels of output.

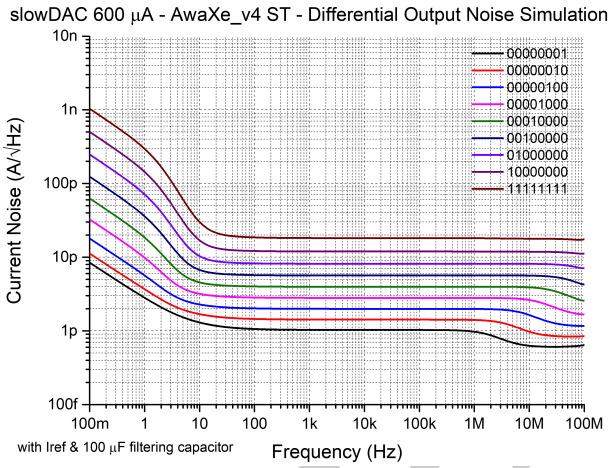

Figure 22: Output current noise of 600 µA DACs, with 9 levels of output.

Drift

The slow DACs were optimised close to 27°C (300 K) around the MSB level in terms of output drift, because the operating level will be close to the MSB instead of extreme values. Figures 23 and 24 show the simulations with the current reference with R_{CTAT} = 2.7 kΩ and R_{PTAT} = 420 Ω (refer to Figure 16) at 3 levels output: maximum output, MSB and LSB. The according drift are listed in Table 5.

Table 5: Simulated output current drift of slow DAC in ASIC "AwaXe_v4"

Output level	Drift of 2.2 mA DAC		Drift of 600 µA DAC	
	17°C	37°C	17°C	37°C
Max output	267 ppm/K	199 ppm/K	324 ppm/K	244 ppm/K
MSB	55 ppm/K	-27 ppm/K	106 ppm/K	17 ppm/K
LSB	-45 ppm/K	-96 ppm/K	71 ppm/K	24 ppm/K

AC Output impedance

Figures 25 and 26 illustrate the simulated AC output impedance of 2.2 mA and 600 µA

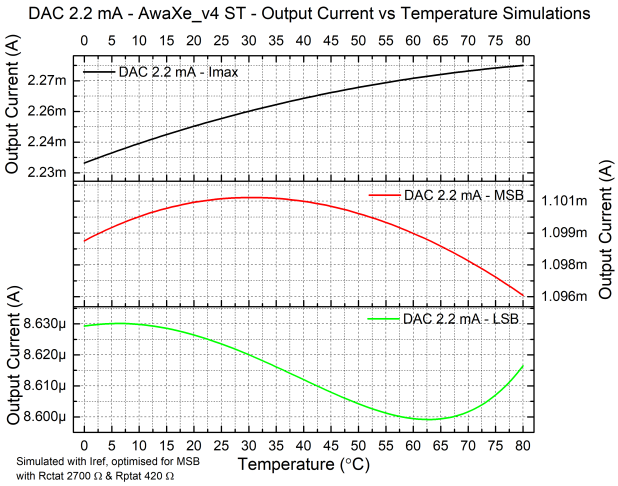

Figure 23: 3 levels of output current (from top to bottom: max, MSB and LSB) of the 2.2 mA DAC vs temperature.

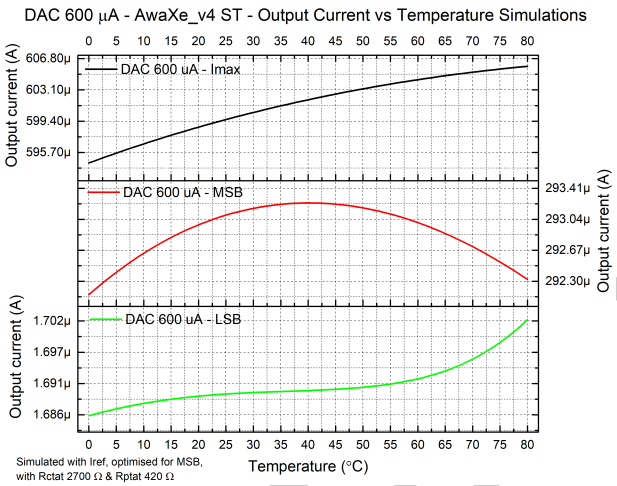

Figure 24: 3 levels of output current (from top to bottom: max, MSB and LSB) of the 600 µA DAC vs temperature.

DACs with 3 levels output: maximum output, MSB and LSB. The source impedance is the output impedance of the PNP BJT output mirror and the sink impedance is of the NPN HBT mirror, thus have different impedances, notably at lower frequencies. According to the simulations, at 20 MHz, the differential output impedance of 2.2 mA DAC is about 1.3 kΩ and that of 600 µA is about 3.47 kΩ.

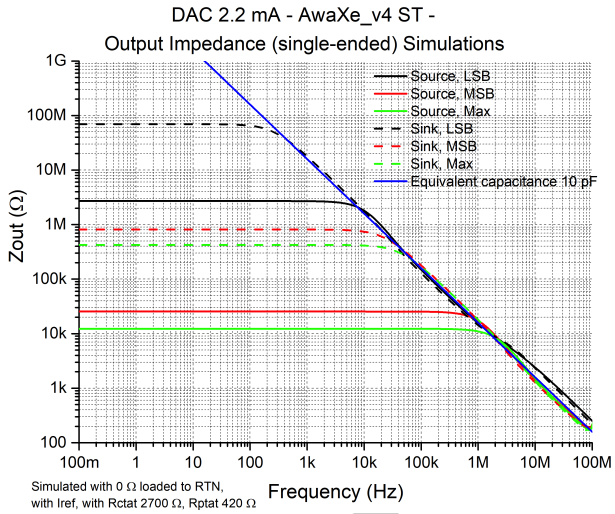

Figure 25: Single-ended output impedance of 2.2 mA DAC vs frequency, with 3 levels of output: LSB, MSB and maximum current. "Source" outputs positive current and "sink" outputs negative current. The parasitic capacitance at both outputs is about 10 pF.

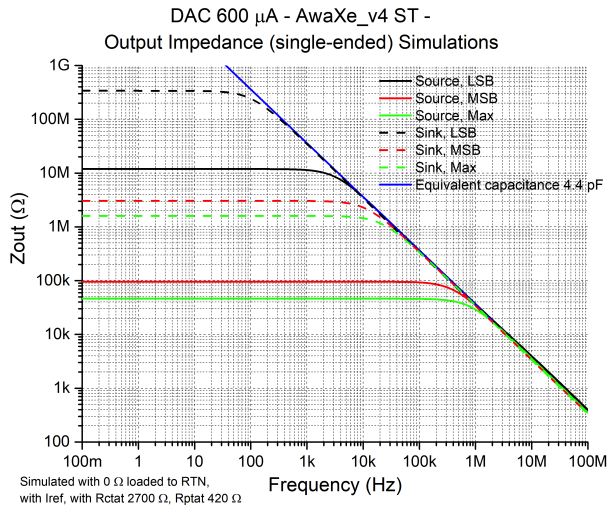

Figure 26: Single-ended output impedance of 600 µA DAC vs frequency, with 3 levels of output: LSB, MSB and maximum current. "Source" outputs positive current and "sink" outputs negative current. The parasitic capacitance at both outputs is about 4.4 pF.

PSRR

Figure 27 shows the AC response of different output current levels LSB, MSB and max of two DACs (2.2 mA and 600 µA) to power supply's fluctuation. The simulations added 1 V AC signal to the power supply V_{CC}.

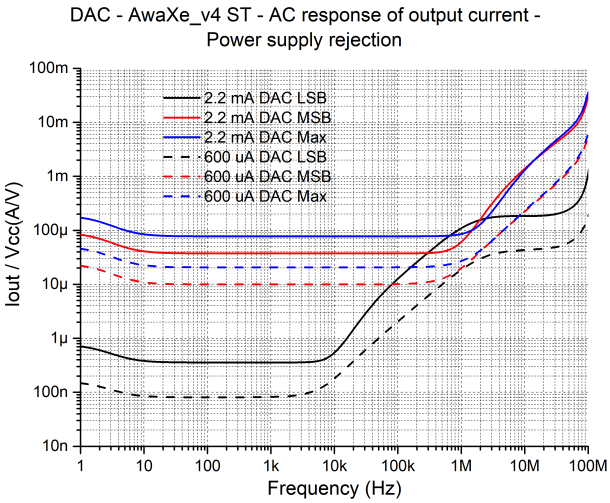

Figure 27: AC response of the output current of DACs to power supply's fluctuation.

CMRR

Figures 28 and 29 show the output current variation of the two DACs (2.2 mA and 600 µA) due to the fluctuation of the common-mode voltage at the output. The V_{cm} of 0 V is 1.65 V higher than V_{EE} = –1.65 V.

According to the simulations, a fluctuation of 0.1 V cause a variation of about 2 kppm for both DAC with MSB and Max output.

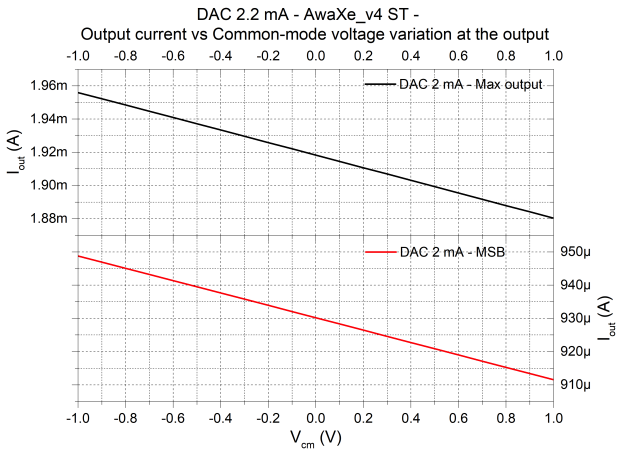

Figure 28: Output current of 2.2 mA DAC vs Common-mode voltage fluctuation at the output.

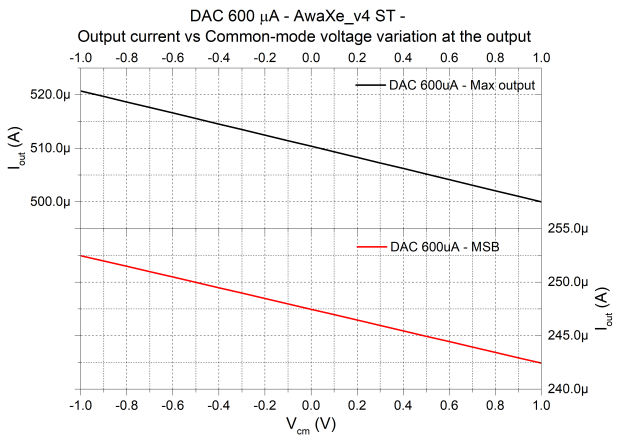

Figure 29: Output current of 600 µA DAC vs Common-mode voltage fluctuation at the output.

Thermometer

BLOCK DIAGRAM

The thermometer (Figure 30) has a pair of differential voltage outputs V_{t+} and V_{t-} (named Vt1 and Vt2 in the pinout). It also has independent complementary and/or proportional-to-temperature bias current. R_{CTAT} is the resistor to adjust the complementary part of the current and R_{PTAT} the one for the current proportional to temperature. R_{PTAT} = 14 kΩ and R_{CTAT} = 700 Ω are validated by simulations.

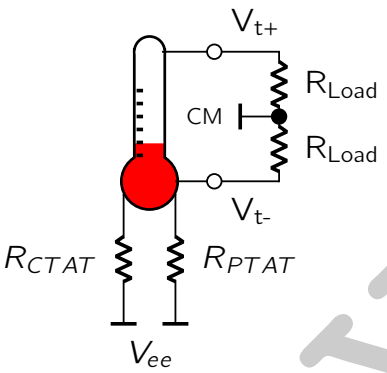

Figure 30: Simplified schematic of the thermometer with basic external connections of resistors. R_{PTAT} = 14 kΩ and R_{CTAT} = 700 Ω, R_{Load} = 4.7 kΩ

If 0 V output voltage is treated as a reference, the temperature corresponds to 0 V can be configured by changing a bit the R_{CTAT} resistance.

Load resistance of 4.7 kΩ is a good trade-off between thermometer sensitivity and wide thermal range.

TYPICAL PERFORMANCE

Simulated differential output voltage as a function of temperature between 10 °C and 80 °C is shown in Figure 31.

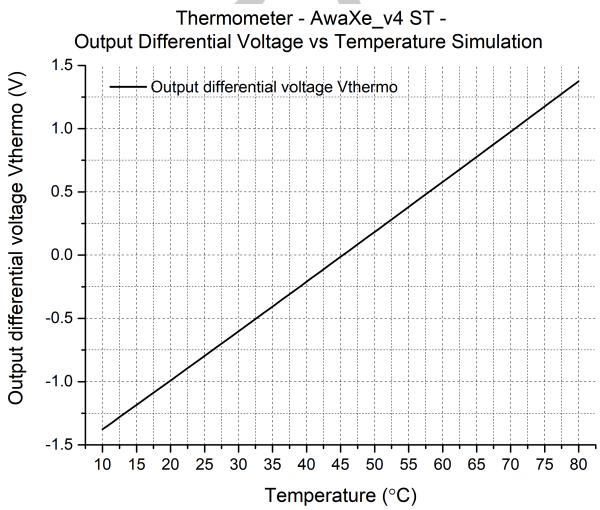

Figure 31: Differential voltage Vt+-Vt- of the thermometer loaded by two 4.7 kΩ resistors connected to Vcm. R_{PTAT}=14 kΩ and R_{CTAT}=700 Ω.

Other devices

Two NPN high-voltage Heterojunction bipolar transistors

The ASIC has integrated a pair of NPN high-voltage(npnvhv) Heterojunction Bipolar Transistors (HBT) for DC and rad-Hard characterisation. As shown in Figure 32, each transistor of the pair is indeed composed of 8 parallel transistors with 5 emitters, 10 bases and 6 collectors with the same dimensions as the ones used in the LNA. The 16 transistors also form a 4×4 common-centroid pattern, the same as a differential pair in the LNA.

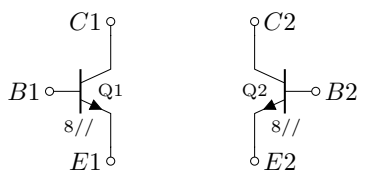

Figure 32: Simplified schematic of the NPN HBT pair.

The simulations shown in Figures 33, 34 and 35 have been done with both transistors connected in parallel. Each of the 16 transistors has 5 emitters of 10 µm length and 0.27 µm of width (fixed value), so the total emitter surface is 10 µm × 0.27 µm ×5 ×16=216 µm^2.

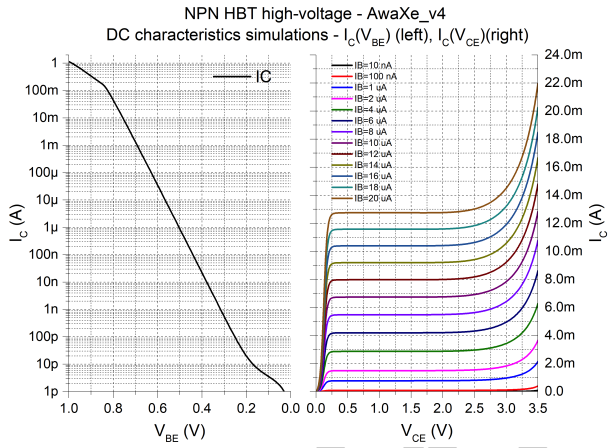

Figure 33: DC characteristics of the NPN HBT. (left) Collector current I_C as a function of V_{BE} (right) Collector current I_C as a function of V_{CE}, corresponding to different levels of base current I_B.

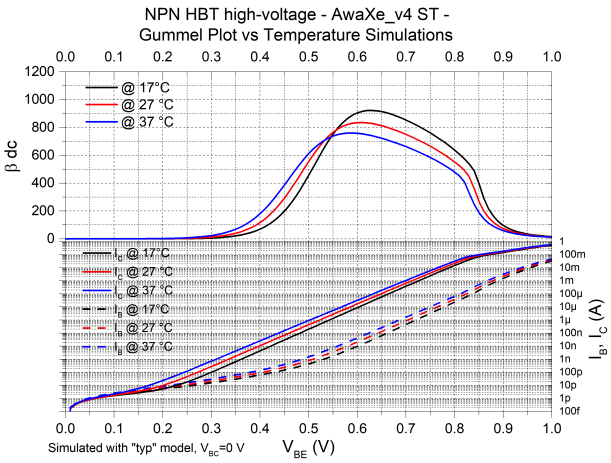

Figure 34: Gummel plot of the NPN HBT at 17°C, 27°C and 37°C. (top) Current gain β. (bottom) Collector current I_C and base current I_B. The total emitter surface is 216 µm^2.

One PNP lateral bipolar transistor

The ASIC has integrated a PNP lateral bipolar transistors (pnpl) for DC and rad-Hard characterisation. The dimension of this type of transistor is unchangeable, with single emitter of 1.2µm ×1.2µm. The transistor integrated into the ASIC is indeed composed of 336 parallel transistors of default dimension, the same number as used in the 1st active load of the LNA. So the total surface of the emitter is 1.2 µm ×1.2 µm × 336=483.84 µm^2.

Figures 36, 37 and 38 show its simulated DC characteristics and Gummel plot. The model does not work very well at very low currents, thus not plotted in the Gummel plots.

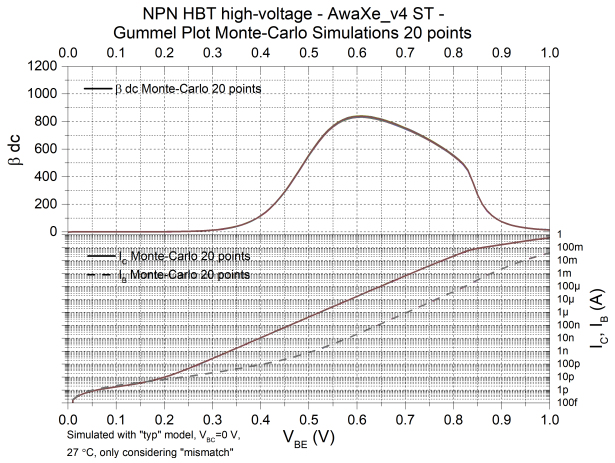

Figure 35: Monte-Carlo simulation 20 points of Gummel plot of the NPN HBT at 27°C. (top) Current gain β. (bottom) Collector current I_C and base current I_B. The total emitter surface is 216 μm^2.

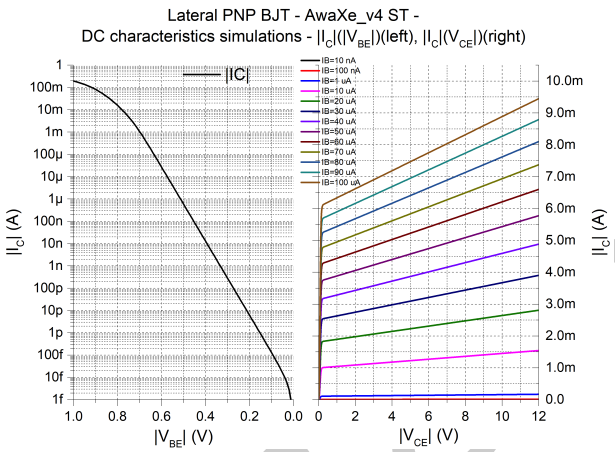

Figure 36: DC characteristics of the PNP lateral BJT. (left) Collector current $|I_C|$ as a function of $|V_{BE}|$ (right) Collector current $|I_C|$ as a function of $|V_{CE}|$, corresponding to different levels of base current I_B.

Two PNP mirrors

The ASIC has integrated two current mirrors of PNP lateral bipolar transistors, aimed to connect to a Digital-to-Analog converter DAC5675A to change the current's direction[5]. As shown in Figure 39, each transistor of the mirrors has indeed 336 transistors in parallel. This number level allows passing a high DC bias current of about 10 mA (a

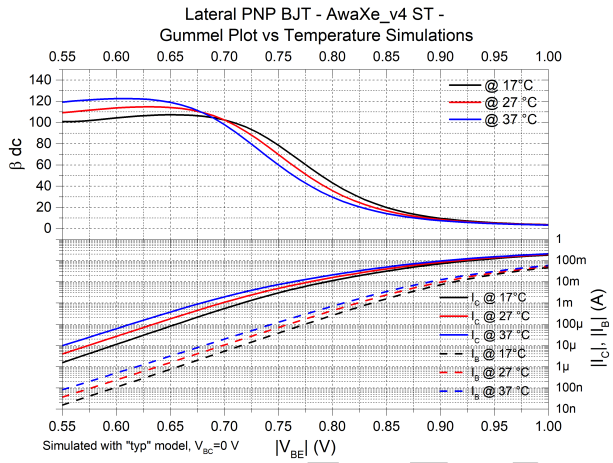

Figure 37: Gummel plot of the PNP BJT at 17°C, 27°C and 37°C. (top) Current gain β. (bottom) Collector current I_C and base current I_B. The total emitter surface is 483.84 μm^2.

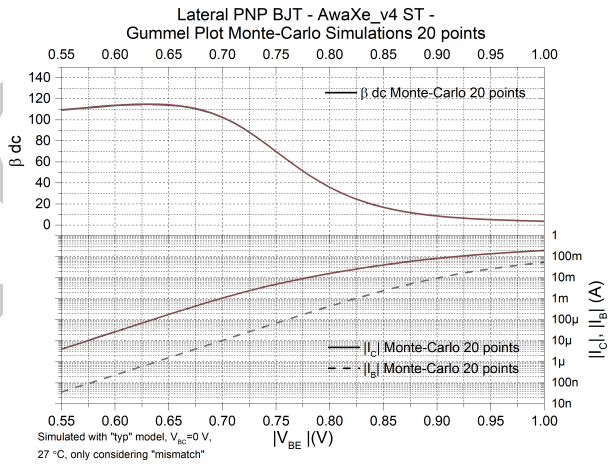

Figure 38: Monte-Carlo simulation 20 points of Gummel plot of the PNP BJT at 27°C. (top) Current gain β. (bottom) Collector current I_C and base current I_B. The total emitter surface is 483.84 μm^2.

[5]DAC5675A included in the Digital Readout Electronics generates the feedback current for SQUIDs. The bias current at the differential outputs of DAC5675A is in the order of about 20 mA, towards V_{CC}. The two PNP mirrors each connecting one output of DAC5675A allow changing current's direction towards V_{ee}

half of 20 mA for the differential outputs of DAC5675A.).

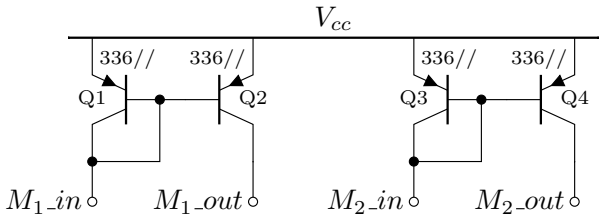

Figure 39: Simplified schematic of the PNP mirrors

Figure 40 shows the AC response of one of the two mirrors.

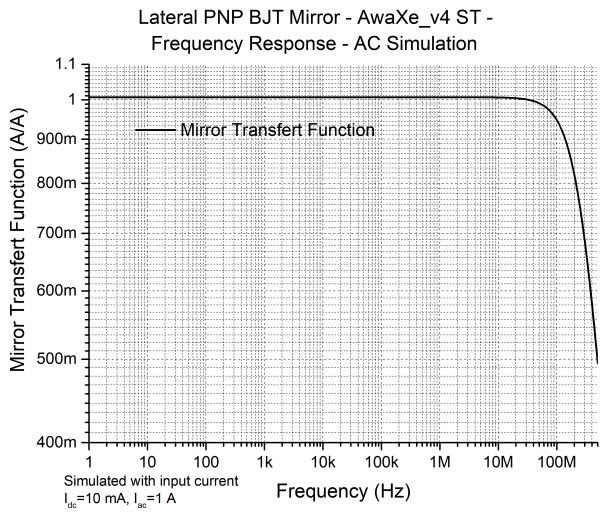

Figure 40: Simulated transfert function vs frequency of the lateral PNP mirror with DC input of 10 mA.

Two NMOS transistors/switches

The ASIC has integrated two high-voltage NMOS transistors (pdomos25) of 2.5 V max for DC and rad-Hard characterisation. They can also be served as a pair of differential switches with the sources as the inputs and the drains as the outputs. The gates are connected together to open/close the switches (Figure 41). The switches are planned to be connected at the inputs of the LNA to isolate the LNA from strong current in the order of 20 mA when SQUIDs need to be heated/defluxed[6].

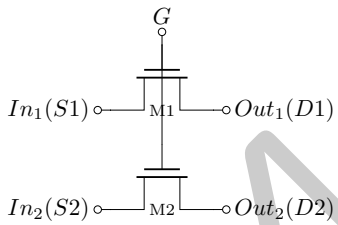

Figure 41: Simplified schematic of the NMOS switch

These two identical NMOS transistors have the same dimensions: L=0.28 µm, W=1 mm (with 2 parallel transistors of W=500 µm). Figure 42 shows the DC characteristics of one of the transistors.

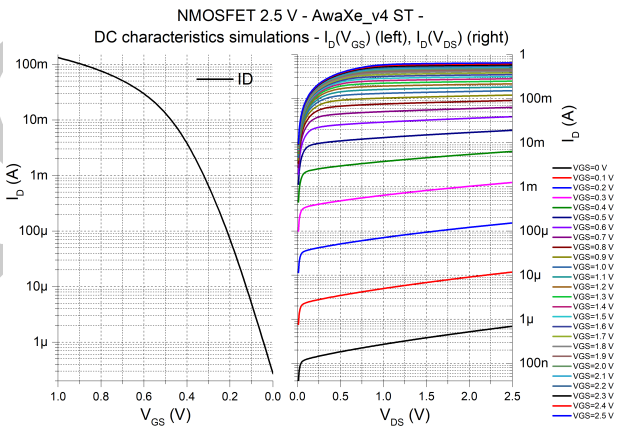

Figure 42: DC characteristics of a 2.5 V NMOS transistor with L=0.28 µm, W=1 mm. (left) $I_D(V_{GS})$; (right) $I_D(V_{DS})$ with different V_{GS} between 0 and 2.5 V.

Functioning as switch, Figure 43 shows the resistance of one of the transistors at open position. Its parasitic capacitance is about 1.14 pF. When at close position, its impedance is about 1.02 Ω constantly from DC up to 100 MHz, thus not shown in the figure.

[6]Without such isolation, part of the heating current will go into the LNA, then lower the efficiency.

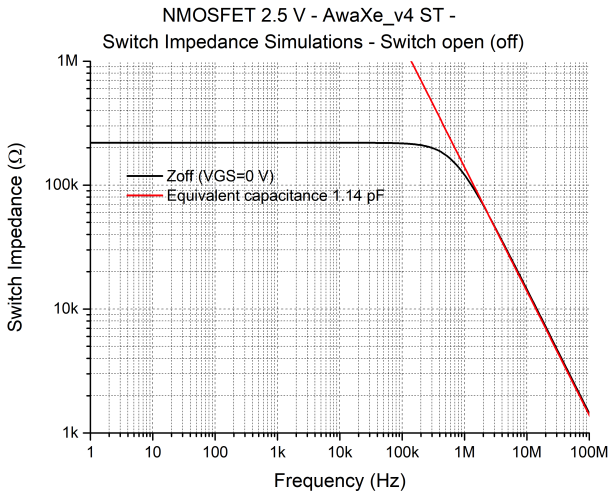

Figure 43: Channel impedance of 2.5 V NMOS transistor operating as a switch at open position (black line). The red line is the equivalent parasitic capacitance of the switch.

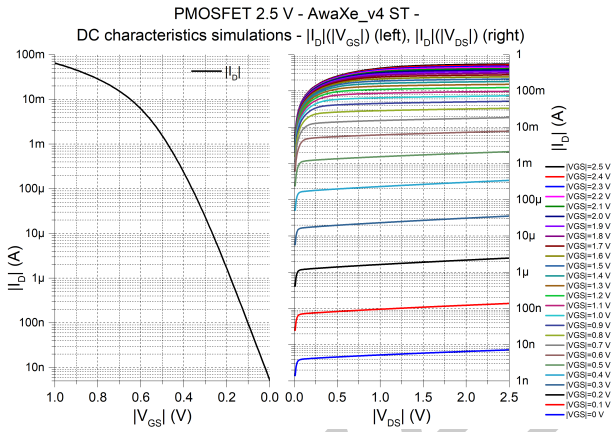

Figure 44: DC characteristics of a 2.5 V PMOS transistor with L=0.28 µm, W=2 mm. (left) $|I_D|(|V_{GS}|)$; (right) $|I_D|(|V_{DS}|)$ with different $|V_{GS}|$ between 0 and 2.5 V.

One PMOS transistor

The ASIC has integrated a high-voltage PMOS transistor (pdomos25) of 2.5 V max for DC and rad-Hard characterisation. The dimensions of the transistor are L=0.28 µm, W=2 mm (with 4 transistors of W=500 µm in parallel).

The simulated DC characterisations are shown in Figure 44.

An N+ Silicided poly resistor

The "Rpolysab" resistor is a type of N+ silicided poly resistor. The LNA has chosen this type for the resistive loop of the first and second stage (R_1, R_2, R_3 and R_4) because its suitable resistance per square (10 Ω/□) and low temperature sensitivity (7.2×10^{-13}).

The ASIC has integrated a resistor of this type with the nominal value of 1248 Ω. Figure 45 shows the drift of resistance as a function of temperature between 0°C and 80°C. The deviation of resistance due to mismatch is illustrated in Figure 46. Figure 47 introduces both mismatch and process.

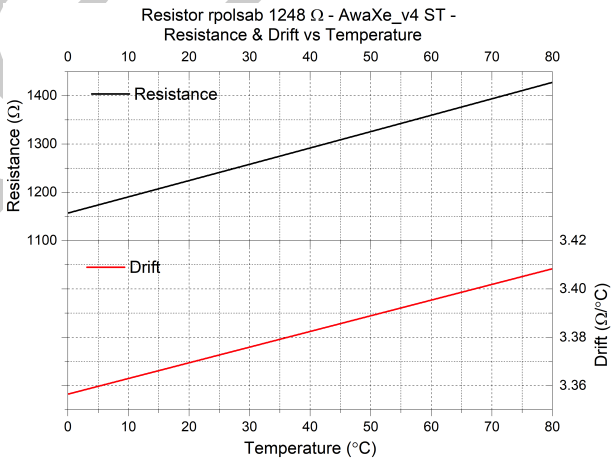

Figure 45: (Top)Resistance as a function of temperature between 0°C and 80°C; (bottom) The drift of resistance

A Metal-Insulator-Metal (MIM) capacitor

The ST 130 nm SiGe BiCMOS technology offers MIM (Metal-Insulator-Metal) capacitors that are not provided by the AMS

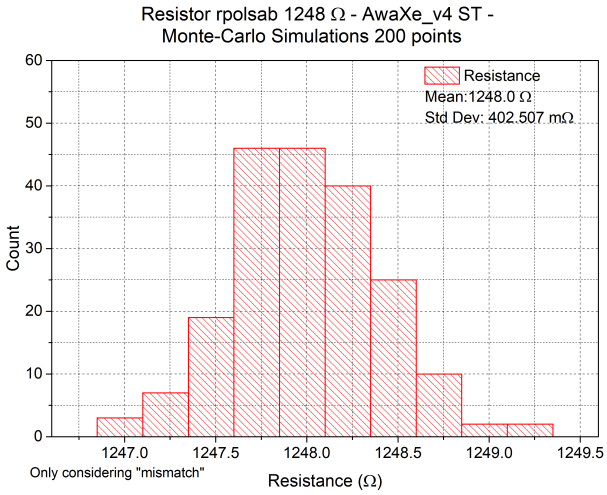

Figure 46: Monte-Carlo simulations of 200 points showing resistance's distribution due to mismatch.

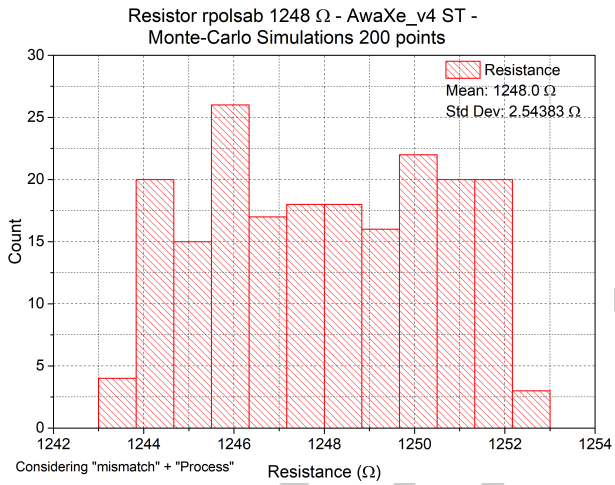

Figure 47: Monte-Carlo simulations of 200 points showing resistance's distribution due to mismatch and process.

350 nm SiGe BiCMOS technology. The capacitor uses layers that are on the top of all 6 metal layers, saving places occupied comparing to poly capacitors. Hence, the ASIC "AwaXe_v4" has massively integrated MIM (Metal-Insulator-Metal) capacitors for the use of reference start-up and decoupling capacitors between V_{cc} and V_{ee}.

A capacitor of nominal 150 pF (6 capacitors of 25 pF in parallel) has been integrated into the ASIC as a single component to be characterised. Figure 48 shows a 200-points Monte-Carlo simulation of capacitance's distribution only considering mismatch. Another 200-points Monte-Carlo simulation further consider both mismatch and process, as shown in Figure **??**.

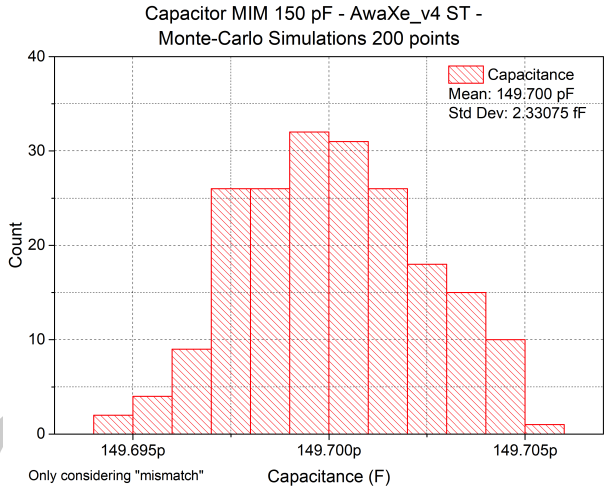

Figure 48: Monte-Carlo simulations of 200 points showing capacitance's distribution due to mismatch.

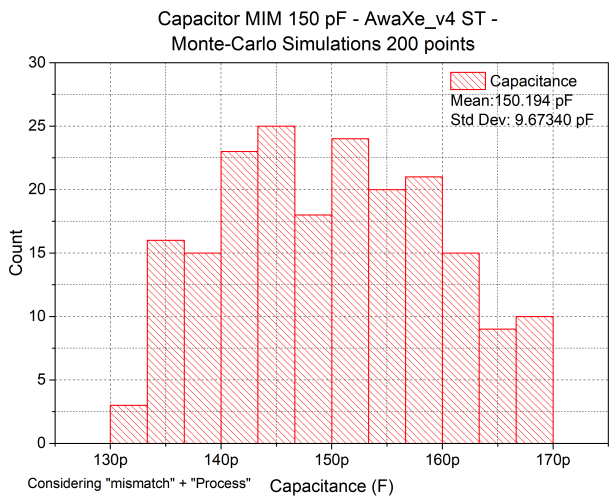

Figure 49: Monte-Carlo simulations of 200 points showing capacitance's distribution due to mismatch and process.

PADs CORRESPONDANCES

This section explains the pinout of the ASIC AwaXe_v4 "bare die". The pinout is also illustrated in Figure 50.

General PADs DESCRIPTIONS

- "gnd" is the "-" power supply V_{ee} of all devices. All the pads "gnd" are connected inside the ASIC with metal layers[7].
- Pads with different names are not electrically connected inside the ASIC.

LNA PADs

The suffix "OS" marks the pads of the LNA with a supplementary measure of offset compensation. The pads without "OS" belongs to the LNA without offset compensation.

- "vcc_LNA(_OS)" is the "+" power supply V_{cc} of the LNAs. Must be +1.65 V. There are 3 pads dedicated to this power supply for each LNA, isolated from the other components. vcc_LNA_OS pads are also isolated from the vcc_LNA pads.
- "R_PTAT_LNA(_OS)" must be connected to "gnd" (V_{ee}) through a resistor. It is a reference resistor to generate the bias current of the "proportional to absolute temperature" current reference attached with the LNA. Typical value 340 Ω.
- "In1_LNA(_OS)" and "In2_LNA(_OS)" are the differential inputs of the LNA. They must be referred to a common mode of about 0 V.
- "Out1_LNA(_OS)" and "Out2_LNA(_OS)" are the differential outputs of the LNA. They are also referred to as a common mode of about 0 V.
- "Offset1_LNA_OS" and "Offset2_LNA_OS" are a pair of pads for compensating the amplified input offset if necessary. To use this function, they should be connected to a DC current source. Typical value: 1.45 mA to compensate an offset of 10 mV at the input.

Current reference PADs

- "vcc_Iref" is the "+" power supply V_{cc} for the current reference. Inside ASIC, it is isolated from other V_{cc} pads. Must be **+1.65 V**[8].
- "R_CTAT_Iref" must be connected to "gnd" (V_{ee}) through a resistor. It is a reference resistor to generate current "complementary proportional to absolute temperature (CTAT)". Typical value **2700** Ω.
- "R_PTAT_Iref" must be connected to "gnd" (V_{ee}) through a resistor. It is a reference resistor to generate current "proportional to absolute temperature (PTAT)". Typical value **420** Ω.
- "Irefx" (x=1, 2, 3 or 4) are the identical outputs of the current reference. Each provides about 2.2 mA

[7] gnd is referring to the minimum voltage of the ASIC corresponding to the 375 µm thick silicon substrate of the entire ASIC. Thus, this is necessarily a common reference of the different parts of the chip, for instance: LNA, DACs and Thermometer.

[8] Referring to the LNA

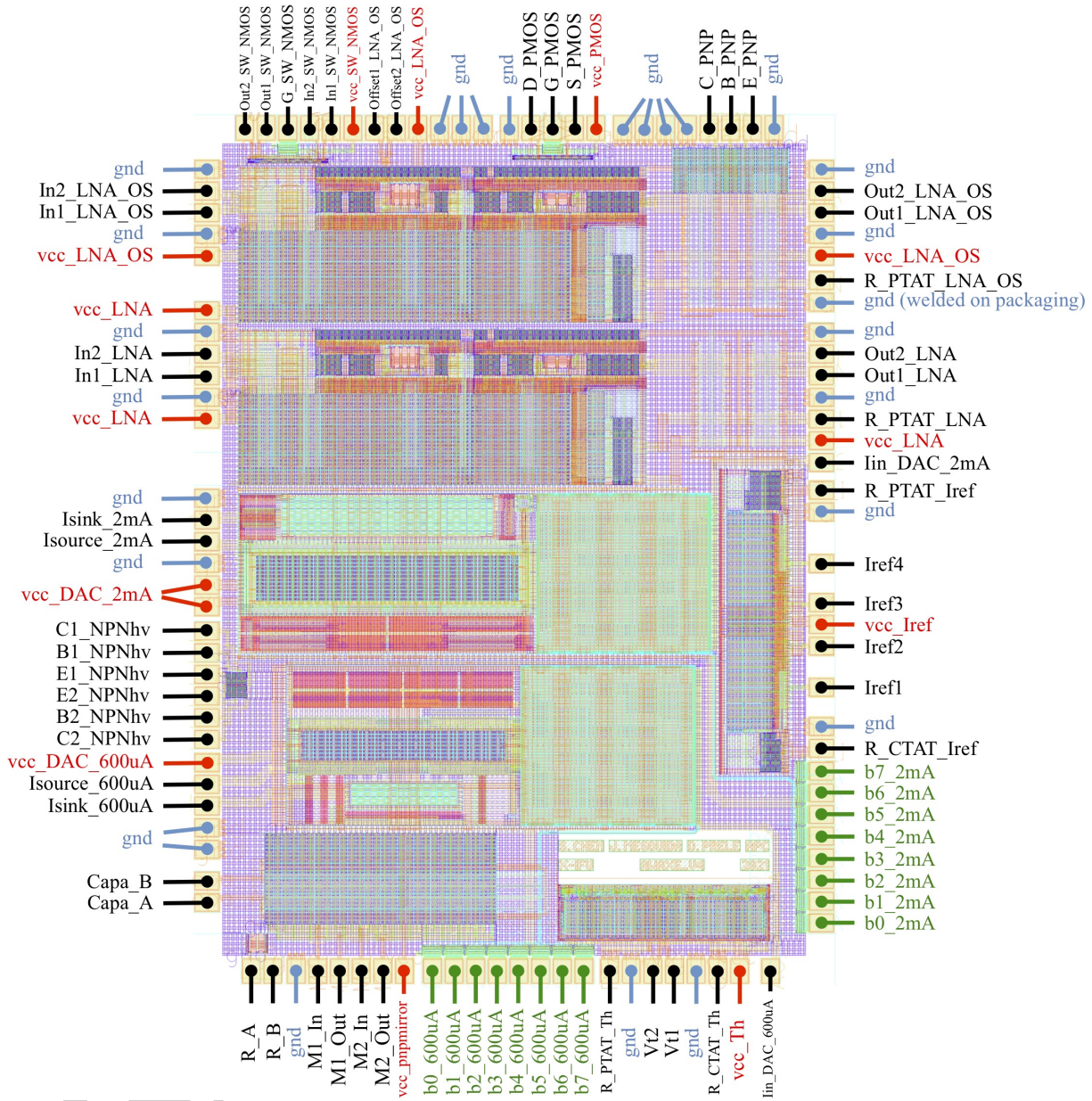

Figure 50: Microscopic photo of AwaXe_v4 at the "bare die" level. Voltage supply V_{cc} = +1.65 V of the devices are independent. However, they can be connected together. All the devices share the same "gnd", that is the lowest potential and should be connected to V_{ee} = -1.65 V. The dice size is about 2014 µm × 2730 µm without seal ring (Complemented by the CMP). Pad pitch = 68 µm.

with the recommended reference resistances and with all 4 outputs are connected. Otherwise, the output level might be different. It must be connected to the pad "Iin_DAC_2mA" or "Iin_DAC_600uA" to bias the slow DACs (to test the current reference and the slow DACs together).

slow DACs PADs

The ASIC integrates two slow DACs with different output current levels: 2.2 mA (max output) and 600 µA (max output). The suffix "2mA" marks the pads of the DAC of 2.2 mA. The suffix "600uA" marks the pads of the DAC of 600 µA.

- "vcc_DAC_2mA" or "vcc_DAC_600uA" are the "+" power supply V_{cc} for the DACs. Electrically, they are not connected together inside the ASIC. The DAC of 2.2 mA has 2 V_{cc} pads, and the DAC of 600 µA has 1 V_{cc} pad. Must be **+1.65 V**[9].
- "bx_2mA" or "bx_600uA" (x = 0, 1, 2, 3, 4, 5, 6 or 7) are the control bits for the DACs. Each DAC has 8 bits. The low level 0 must be V_{ee} of -1.65 V. The high level 1 can be taken between 2-2.5 V.
- "Iin_DAC_2mA" or "Iin_DAC_600uA" are the current inputs of the DACs. They must be connected to one of the 4 outputs of the current reference of the ASIC. It allows connecting a large-value low-pass capacitor on PCB, helping to filter the noises from the reference. Using a 100 µF capacitor with an 825 Ω resistor allows filtering noises down to ≈2 Hz.
- "Isink_2mA" and "Isink_600uA" are the outputs of the DACs that provide negative current.
- "Isource_2mA" and "Isource_600uA" are the outputs of the DACs that provide positive current. The DACs are differential, capable of providing at the same time negative and positive current.

THERMOMETER PADs

- "vcc_Th" is the "+" power supply V_{cc} of the thermometer. Must be +1.65 V[10].
- "R_CTAT_Th" must be connected to "gnd" (V_{ee}) through a resistor. It is a reference resistor to generate current "complementary proportional to absolute temperature (CTAT)". Typical value 700 Ω.
- "R_PTAT_Th" must be connected to "gnd" (V_{ee}) through a resistor. It is a reference resistor to generate current "proportional to absolute temperature (PTAT)". Typical value 14 kΩ.
- Vt1 and Vt2 are the differential outputs of the thermometer. They are in fact a pair of differential current outputs which must be loaded by resistors (R_{Load}, see Figure 30) referred to any common mode in the range [V_{ee}-V_{cc}]. R_{Load} resistors can be placed very (1) near the chip or (2) near the equipment used to measure Vt. Both solutions work. The first one allows minimising the effect of the temperature sensitivity of the load resistors themselves because they roughly follow the ASIC temperatures. The second solution allows to minimise the common

[9] Referring to the LNA

[10] Referring to the LNA

mode coupling because of the very high output impedance of these thermometer outputs consequently only referred to voltage to the measurement equipment.

Other PADs

- "Cx_NPNhv" (x=1 or 2) are the pads connected to the collector of the two high-voltage NPN heterojunction bipolar transistors in the ASIC.
- "Bx_NPNhv" (x=1 or 2) are the pads connected to the base of the two high-voltage NPN heterojunction bipolar transistors in the ASIC.
- "Ex_NPNhv" (x=1 or 2) are the pads connected to the emitter of the two high-voltage NPN heterojunction bipolar transistors in the ASIC.
- "C_PNP" is the pad connected to the collector of the lateral PNP bipolar transistor in the ASIC.
- "B_PNP" is the pad connected to the base of the lateral PNP bipolar transistor in the ASIC.
- "E_PNP" is the pad connected to the emitter of the lateral PNP bipolar transistor in the ASIC.
- "vcc_pnpmirror" is the "+" power supply V_{cc} of the two PNP current mirrors in the ASIC, directly connected to the source of PNP transistors. Must be +1.65 V[11].
- "Mx_In" (x=1 or 2) are the input pads of the two PNP current mirrors in the ASIC.
- "Mx_Out" (x=1 or 2) are the output pads of the two PNP current mirrors in the ASIC.
- "vcc_SW_NMOS" is the "+" power supply V_{cc} connected to a diode to protect the gate from Electro-Static Discharge. Must be no higher than 0.85 V.
- "Inx_SW_NMOS" (x=1 or 2) are the pads connected to the source of the two 2.5 V NMOS transistors in the ASIC, that can also be used as the differential inputs of the switches for the LNA.
- "Outx_SW_NMOS" (x=1 or 2) are the pads connected to the drain of the two 2.5 V NMOS transistors in the ASIC. When used as the differential outputs of the switches, they must be connected to the inputs of the LNA.
- "G_SW_NMOS" is the pad connected to both gates of the two 2.5 V NMOS transistors in the ASIC, that can also be used as the control of the switches for the LNA.
- "vcc_PMOS" is the "+" power supply V_{cc} to bias the n-well. It is also connected to a diode to protect the gate from Electro-Static Discharge. Must be no higher than 0.85 V.
- "D_PMOS" is the pad connected to the drain of the 2.5 V PMOS transistor in the ASIC.
- "G_PMOS" is the pad connected to the gate of the 2.5 V PMOS transistor in the ASIC.
- "S_PMOS" is the pad connected to the source of the 2.5 V PMOS transistor in the ASIC.
- "Capa_A" and "Capa_B" are the pads connected to the two terminals of the

[11] Referring to the LNA

"MIM" type capacitor of 150 pF in the ASIC.

- "R_A" and "R_B" are the pads connected to the two terminals of the "Rpolysab" type resistor of 1248 Ω in the ASIC.

PACKAGE DESCRIPTION

The ASIC AwaXe_v4 can either be provided as a bare-die or packaged in **CQFP120Z**[12]. The bonding diagram of the packaging is shown in Figure 51, following Table 6 listing the pinout. The pins names are kept the same as the bare-die level. Users can refer to the section "PADs CORRESPONDANCES" for the descriptions in case of needs.

PIN FUNCTIONS

Table 6: CQFP120 Pinout

No.	Name	Type	Description
1	R_A	Component	1st pin of an integrated resistor of 1248 Ω
2	R_B	Component	2nd pin of an integrated resistor of 1248 Ω
3	nc		
4	gnd	Power supply	Global Vee -1.65 V
5	M1_In	Signal	1st pnp mirror's Input
6	M1_Out	Signal	1st pnp mirror's Output
7	nc		
8	M2_In	Signal	2nd pnp mirror's Input
9	M2_Out	Signal	2nd pnp mirror's Output
10	vcc_pnpmirror	Power supply	Vcc 1.65 V, only for the two pnp mirrors
11	nc		
12	b0_600uA	Digital binary bit	To configure the DAC of 600 µA, LSB
13	b1_600uA	Digital binary bit	To configure the DAC of 600 µA
14	b2_600uA	Digital binary bit	To configure the DAC of 600 µA
15	b3_600uA	Digital binary bit	To configure the DAC of 600 µA
16	b4_600uA	Digital binary bit	To configure the DAC of 600 µA
17	b5_600uA	Digital binary bit	To configure the DAC of 600 µA
18	b6_600uA	Digital binary bit	To configure the DAC of 600 µA
19	b7_600uA	Digital binary bit	To configure the DAC of 600 µA, MSB
20	nc		
21	R_PTAT_Th	DC	To connect the PTAT reference's resistor of the thermometer
22	gnd	Power supply	Global Vee -1.65 V
23	Vt2	Signal	Differential voltage output of the thermometer
24	Vt1	Signal	Differential voltage output of the thermometer
25	gnd	Power supply	Global Vee -1.65 V
26	R_CTAT_Th	DC	To connect the CTAT reference's resistor of the thermometer
27	vcc_Th	Power supply	Vcc 1.65 V, only for the thermometer
28	nc		
29	Iin_DAC_600uA	DC	To input current for the DAC of 600 µA
30	nc		
31	b0_2mA	Digital binary bit	To configure the DAC of 2.2 mA, LSB
32	b1_2mA	Digital binary bit	To configure the DAC of 2.2 mA
33	b2_2mA	Digital binary bit	To configure the DAC of 2.2 mA
34	b3_2mA	Digital binary bit	To configure the DAC of 2.2 mA
35	b4_2mA	Digital binary bit	To configure the DAC of 2.2 mA
36	b5_2mA	Digital binary bit	To configure the DAC of 2.2 mA
37	b6_2mA	Digital binary bit	To configure the DAC of 2.2 mA
38	b7_2mA	Digital binary bit	To configure the DAC of 2.2 mA, MSB
39	R_CTAT_Iref	DC	To connect the CTAT reference's resistor of the current reference
40	gnd	Power supply	Global Vee -1.65 V
41	Iref1	DC	1st output current of 2.2 mA of the current reference
42	Iref2	DC	2nd output current of 2.2 mA of the current reference
43	vcc_Iref	Power supply	Vcc 1.65 V, only for the current reference
44	Iref3	DC	3rd output current of 2.2 mA of the current reference
45	Iref4	DC	4th output current of 2.2 mA of the current reference
46	gnd	Power supply	Global Vee -1.65 V
47	R_PTAT_Iref	DC	To connect the PTAT reference's resistor of the current reference
48	Iin_DAC_2mA	DC	To input current for the DAC of 2.2 mA
49	vcc_LNA	Power supply	Vcc 1.65 V, only for the LNA without offset compensation
50	R_PTAT_LNA	DC	To connect the PTAT reference's resistor of the LNA without offset compensation
51	gnd	Power supply	Global Vee -1.65 V
52	Out1_LNA	Signal	Differential voltage output of the LNA without offset compensation
53	Out2_LNA	Signal	Differential voltage output of the LNA without offset compensation
54	gnd	Power supply	Global Vee -1.65 V
55	R_PTAT_LNA_OS	DC	To connect the PTAT reference's resistor of the LNA with offset compensation
56	vcc_LNA_OS	Power supply	Vcc 1.65 V, only for the LNA with offset compensation
57	gnd	Power supply	Global Vee -1.65 V
58	Out1_LNA_OS	Signal	Differential voltage output of the LNA with offset compensation
59	Out2_LNA_OS	Signal	Differential voltage output of the LNA with offset compensation
60	gnd	Power supply	Global Vee -1.65 V
61	gnd	Power supply	Global Vee -1.65 V
62	E_PNP	Component	Emitter of the pnp bipolar transistor (336//)
63	B_PNP	Component	Base of the pnp bipolar transistor (336//)
64	C_PNP	Component	Collector of the pnp bipolar transistor (336//)
65	gnd	Power supply	Global Vee -1.65 V
66	gnd	Power supply	Global Vee -1.65 V
67	gnd	Power supply	Global Vee -1.65 V
68	gnd	Power supply	Global Vee -1.65 V
69	nc		
70	vcc_PMOS	Power supply	For the ESD protection of the gate of the PMOS transistor and the bias of n-well, 0.85 V max.
71	S_PMOS	Component	Source of the PMOS transistor
72	G_PMOS	Component	Gate of the PMOS transistor
73	D_PMOS	Component	Drain of the PMOS transistor
74	gnd	Power supply	Global Vee -1.65 V
75	nc		
76	gnd	Power supply	Global Vee -1.65 V
77	gnd	Power supply	Global Vee -1.65 V
78	gnd	Power supply	Global Vee -1.65 V
79	nc		
80	vcc_LNA_OS	Power supply	Vcc 1.65 V, only for the LNA with offset compensation
81	nc		
82	Offset2_LNA_OS	Signal & DC	To connect DC current for the offset compensation of the LNA
83	Offset1_LNA_OS	Signal & DC	To connect DC current for the offset compensation of the LNA
84	nc		
85	vcc_SW_NMOS	Power supply	Only for the ESD protection of the gate of the NMOS switches/transistors
86	In1_SW_NMOS	Signal	Input/Source of the 1st NMOS switch/transistor
87	In2_SW_NMOS	Signal	Input/Source of the 2nd NMOS switch/transistor
88	G_SW_NMOS	Signal	Control/Gate of both NMOS switches/transistors
89	Out1_SW_NMOS	Signal	Output/Drain of the 1st NMOS switch/transistor

[12] Ceramic Quad Flat Pack of 120 pins bent in gull wing

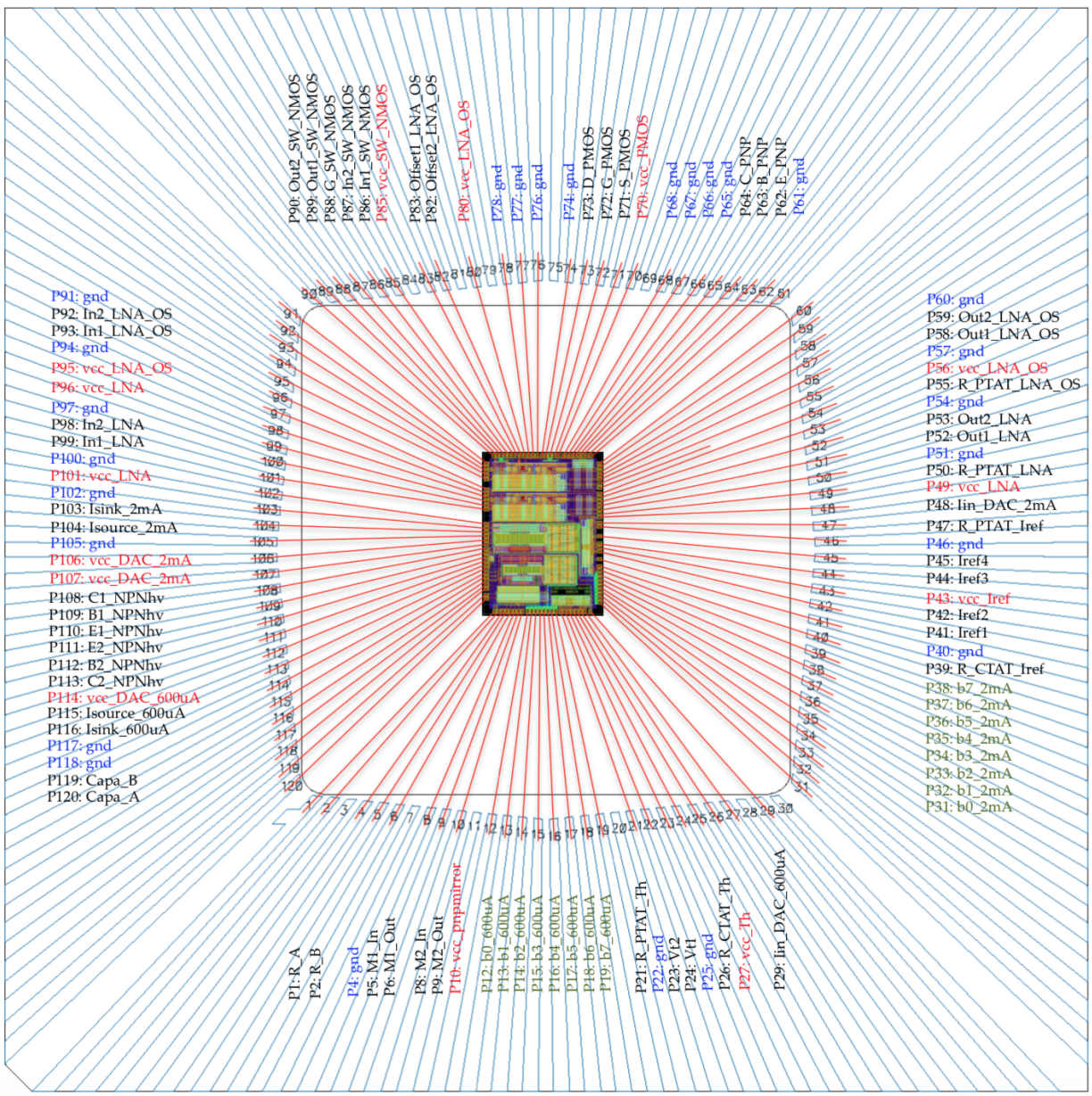

Figure 51: CQFP 120 bonding diagram and Pin connections. Pin 1 and 120 are on the bottom left. Not connected pins can be left open or connected to Vee (preferred for thermal and EMC reasons)

90	Out2_SW_NMOS	Signal	Output/Drain of the 2nd NMOS switch/transistor
91	gnd	Power supply	Global Vee -1.65 V
92	In2_LNA_OS	Signal	Differential voltage input of the LNA with offset compensation
93	In1_LNA_OS	Signal	Differential voltage input of the LNA with offset compensation
94	gnd	Power supply	Global Vee -1.65 V
95	vcc_LNA_OS	Power supply	Vcc 1.65 V, only for the LNA with offset compensation
96	vcc_LNA	Power supply	Vcc 1.65 V, only for the LNA without offset compensation
97	gnd	Power supply	Global Vee -1.65 V
98	In2_LNA	Signal	Differential voltage input of the LNA without offset compensation
99	In1_LNA	Signal	Differential voltage input of the LNA without offset compensation
100	gnd	Power supply	Global Vee -1.65 V
101	vcc_LNA	Power supply	Vcc 1.65 V, only for the LNA without offset compensation
102	gnd	Power supply	Global Vee -1.65 V
103	Isink_2mA	DC Signal	Negative current output of the DAC of 2.2 mA
104	Isource_2mA	DC Signal	Positive current output of the DAC of 2.2 mA
105	gnd	Power supply	Global Vee -1.65 V
106	vcc_DAC_2mA	Power supply	Vcc 1.65 V, only for the DAC of 2.2 mA
107	vcc_DAC_2mA	Power supply	Vcc 1.65 V, only for the DAC of 2.2 mA
108	C1_NPNhv	Component	Collector of the 1st NPN high voltage HBT (8//)
109	B1_NPNhv	Component	Base of the 1st NPN high voltage HBT (8//)
110	E1_NPNhv	Component	Emitter of the 1st NPN high voltage HBT (8//)
111	E2_NPNhv	Component	Emitter of the 2nd NPN high voltage HBT (8//)
112	B2_NPNhv	Component	Base of the 2nd NPN high voltage HBT (8//)
113	C2_NPNhv	Component	Collector of the 2nd NPN high voltage HBT (8//)
114	vcc_DAC_600uA	Power supply	Vcc 1.65 V, only for the DAC of 600 μA
115	Isource_600uA	DC Signal	Positive current output of the DAC of 600 μA
116	Isink_600uA	DC Signal	Negative current output of the DAC of 600 μA
117	gnd	Power supply	Global Vee -1.65 V
118	gnd	Power supply	Global Vee -1.65 V
119	Capa_B	Component	2nd pin of an integrated MIM capacitor of 150 pF
120	Capa_A	Component	1st pin of an integrated MIM capacitor of 150 pF

APPLICATION - TYPICAL USE

Power supply

All the devices, except NMOSFET and PMOSFET, must respect the following bias conditions to function correctly:

- V_{cc} = 1.65 V
- V_{cm} = 0 V
- V_{ee} = -1.65 V

The voltage room between V_{cc} and V_{ee} is 3.3 V. V_{cm} is the bias voltage needed for the base of the front-end bipolar transistors, thus referred to the **common mode** of the differential input signal. Different from the old versions of "AwaXe", the V_{cm} of this ASIC is right in the middle, thus takes the ground of 0 V. Then, V_{cc} and V_{ee} are simply generated with two power supply of 1.65 V, as shown in Figure 52. Diode such as "PMEG6010CEH,115" is recommended to prevent ESD discharge, overvoltage, spike and/or inversion during power supply connections. Capacitors of 10 µF and 100 nF are proposed between supply lines to filter noises.

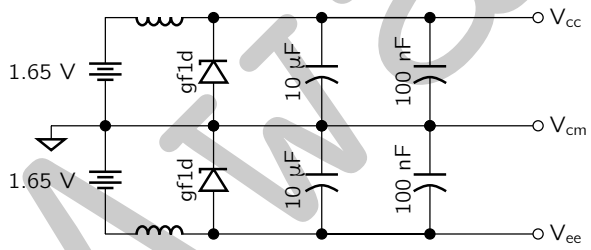

Figure 52: Proposed schematic to generated power supplies V_{cc}, V_{cm} and V_{ee}.

Power supply for components MOSFET

For the MOSFETs in the ASIC, the power supply must respect the following two conditions to protect the components and function correctly:

- V_{dd} = 0.85 V
- V_{ss} = -1.65 V

The voltage room between V_{dd} and V_{ss} is 2.5 V. A 2.5 V voltage regulator "LP2985IM5-2.5" or "TC1185-2.5VCT713" is recommended to generate the power supply for the MOS transistors, as shown in Figure 53.

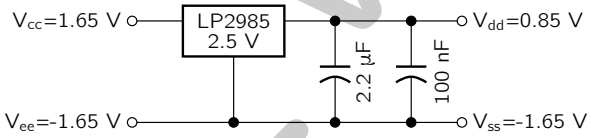

Figure 53: Proposed schematic to generated power supplies V_{dd} and V_{ss} for the MOS transistors.

Power supply decoupling philosophy

The power supply V_{cc} of each component is isolated from the others inside the ASIC. To prevent any disturbance from one system to the other, each device should equip a dedicated capacitor bank. Although a very large capacitance can theoretically filter down to very low frequency, parasitic resistances and inductances will degrade the filtering effect at a higher frequency range. Hence, 3 capacitors respectively in the order of a few µF, 100 nF and 1 nF are recommended to be used in parallel, as shown in Figure 54. Assuming that a larger capacitance causes a larger equivalent series resistance (ESR), it is better to place the smallest capacitors as close as possible to the ASIC.

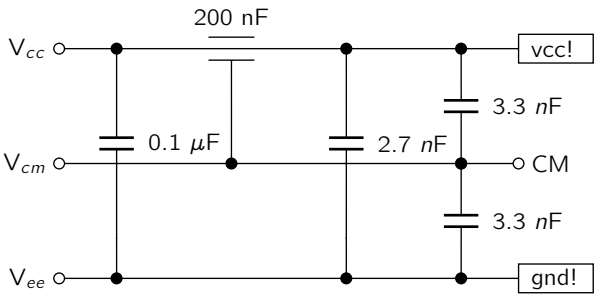

Figure 54: Proposed power supply filtering using a bank of 3 capacitors between every two voltages. 22 µF or 10 µF MLCC X5R or Tantal 10 V + 100 nF 100 V COG. or 200 nF 50 V three terminal capacitors NFM41p + 2.7 or 3.3 nF 25 V MLCC COG. The "vcc!" and "gnd!" on the right side represent the pads of the ASIC. The "V_{cc}", "V_{cm}" and "V_{ee}" are the power supply connections.

PCB - Evaluation boards

Power supply

As mentioned in the previous section, the PCB should connect to ±1.65 V to power the whole board (Figure 52). For the MOS transistors enduring less voltage room of 2.5 V, a voltage regulator "LP2985IM5-2.5" or "TC1185-2.5VCT713" is recommended, as shown in Figure 53. To filter the power supplies of each component, a bank of capacitors is proposed as shown in Figure 54.

LNA

Figure 55 shows the connections on PCB for characterising the LNA. Its differential inputs and outputs directly connect to a common-mode filter (CMF: "ACP3225-102-2P-T000"), which improves the common-mode noise rejection and the symmetry of the signals. Differential diodes "MMBZ9V1ALT1G" protect the differential input and output of any over-voltages (ESD suppressor). Such diodes should also be used between any other differential lines: between "Isource_600uA" and "Isink_600uA", between "Isource_2mA" and "Isink_2mA" of the two slow DACs, between "Vt1" and "Vt2" of the thermometer.

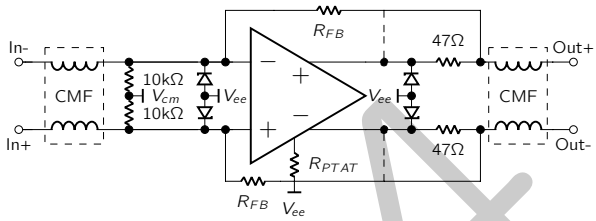

Figure 55: Schematic showing the discrete devices implemented on the evaluation board to operate the LNA. Common-mode filters (CMF: ACP3225-102-2P-T000) to improve symmetry and to reject common-mode noise; ESD suppressor diodes (MMBZ9V1ALT1G) at the input and the output avoiding any over-voltages; 10 kΩ resistors to bias the bases of the input transistors ($I_b \approx 7$ µA); Two 47 Ω resistors (with an intrinsic differential output impedance of about 6 Ω) to match a 100 Ω line at the output; A 340 Ω resistor R_{PTAT} is needed to generate bias current and helps to minimise gain drift; Feedback resistors $R_{FB} \approx 8350$ Ω to achieve input matching.

The common-mode input bias of the LNA uses two 10 kΩ resistors connected to V_{cm} (0 V). With $I_b = \frac{I_C}{\beta} \approx 7$ µA, the voltage drop of about 70 mV can be considered negligible at the input of the LNA. The noise contribution of about 10 nV/$\sqrt{\text{Hz}}$ of these 10 kΩ resistors is strongly attenuated by the voltage bridge divider formed by the 10 kΩ itself and the source impedance: Assuming 200 Ω source resistance, the 10 nV/$\sqrt{\text{Hz}}$ Johnson noise contribution is finally reduced by about two orders of magnitude, meaning about 100 pV/$\sqrt{\text{Hz}}$ which is significantly less than the LNA intrinsic noise.

The input impedance of the open-loop is about 8 kΩ. Input matching is achieved using feedback resistors R_{FB}.

R_{FB} emulates a Miller input impedance of about $R_{FB}/\text{Gain}_{\text{Open-loop}}$, where the in-

trinsic open-loop gain of the LNA is about 160 V/V. However, if including the two 47 Ω resistors in the loop (dashed connections in Figure 55), $Gain_{Open-loop}$ becomes a half, about 80 V/V. Hence, the value of R_{FB} depends on the source resistance to be matched and where to connect the R_{FB} resistors at the output, as listed in Table 7.

Table 7: R_{FB}'s values

Source differential impedance	Output connection position	R_{FB}
100 Ω	Before 47 Ω resistors	8350 Ω
100 Ω	Atter 47 Ω resistors	4175 Ω
200 Ω	Before 47 Ω resistors	16700 Ω
200 Ω	Atter 47 Ω resistor	8350 Ω

The LNA intrinsic differential output impedance equals about 6 Ω ($2k_BT/qIc$). The output matching is obtained by adding extra 47 Ω resistors in series with outputs, to adapt 100 Ω load.

A 340 Ω R_{PTAT} resistor is used to generate a bias current. The current is proportional to absolute temperature, allowing to minimise gain drift (compensating the decrease of the transconductance with temperature). However, the value of R_{PTAT} needs to be verified by measuring the voltage at the edge of R_{PTAT}, which needs to be about 58 mV, before operating the LNA.

Current reference and slow DAC

The current reference requires a resistor R_{CTAT} of 2.7 kΩ and an R_{PTAT} of 420 Ω to minimise the drift of output current of slow DACs at MSB level around 300 K. Yet, the values need to be verified. If the minimum drift (≈0) is at a higher temperature, users need to increase a little R_{CTAT} and decrease a little R_{PTAT}. Vice versa.

The input of slow DACs needs to connect to one of the outputs of the current reference. "Iref1" and "Iref2" are reserved for the two DACs. Three capacitors of 100 μF, 100 nF and 1-10 nF with a resistor of about 800 Ω allow filtering the output current noise of the reference down to lower than 10 Hz. An optional tantalum capacitor "TPSV108K004R0035" of 1 mF can also be added to further cut off the noise.

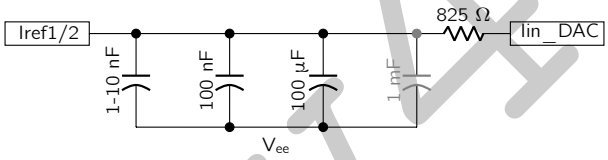

Figure 56: RC filters between the outputs of the current reference "Iref1" or "Iref2" and the input of slow DACs. The optional 1 mF tantalum capacitor can choose "TPSV108K004R0035".

"Iref3" and "Iref4" are reserved to measure the output current and noise of the reference. The output "Iref3" is also connected with the same capacitor bank of "Iref1" or "Iref2", so its noise is filtered. The output "Iref4" has no capacitor connected, with unfiltered noise.

The differential outputs of slow DACs adopt the same connections as the LNA, as shown in Figure 57, with differential diodes "MMBZ9V1ALT1G" and common-mode filters (CMF: ACP3225-102-2P-T000).

The 8 control bits of slow DACs must use -1.65 V as "0" and 0.85 V as "1".

Thermometer

The thermometer requires a resistor R_{CTAT} of 700 Ω and an R_{PTAT} of 14 kΩ.

Similar to the LNA and the slow DACs, the differential outputs of the thermometer also need to be protected with differential diodes "MMBZ9V1ALT1G" and biased with two 10 kΩ resistors connected to V_{ee}, as shown in Figure 58.

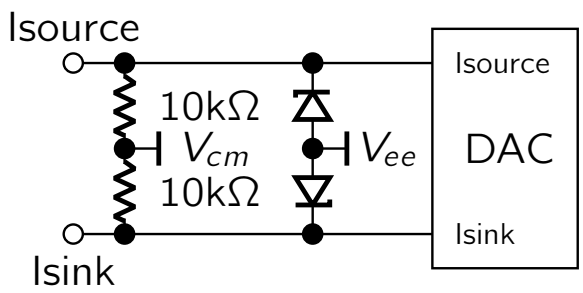

Figure 57: Connections of the differential outputs of slow DACs, with differential diodes "MMBZ9V1ALT1G" and common-mode filters (CMF: ACP3225-102-2P-T000).

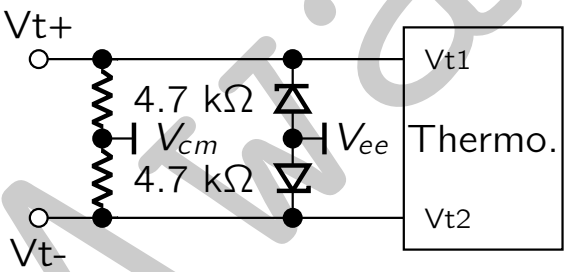

Figure 58: Connections of the differential outputs of the thermometer, using differential diodes "MMBZ9V1ALT1G".

ESD CAUTION

ASICs are ESD (Electro-Static Discharge) sensitive devices. The human body and test equipment readily accumulate electrostatic charges as high as few kV that may discharge without detection. Although many protections exist in the chip and on the proposed evaluation board, proper ESD precautions should be taken to avoid performance degradations, loss of functionalities or any other damage which may occur on devices subjected to high energy ESD.

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VERSION

- Version 1.0, 22/11/2021