Double Channels WFEE

Two **Low-noise amplifiers** (one per channel) fully differential, low-gain drift and high linearity
+ ten **quasi-DC current sources adjustable** (5 per channel, configured via 8-bit SlowDAC) through a differential I^2C/RS485 Bus.
+ an **On-Chip Thermometer**, a **current monitoring** module and **voltage monitoring** pads.

FEATURES

2 Differential voltage LNAs (1/CH)

- **Voltage gain** 170 V/V (intrinsic); 85 V/V (loaded)
- **Voltage noise** < 1 nV/$\sqrt{\text{Hz}}$ @ f > 100 Hz
- **Current noise** 2-3 pA/$\sqrt{\text{Hz}}$
- **Gain drift** 100-500 ppm/K
- **Bandwidth** DC-17.5 MHz (-1 dB)
- **Slew rate** 25 V/μs @ 1 MHz 1 V_{pp}
- **High PSRR** > 80 dB @ V_{ICM} = 0 V
- **High CMRR** > 100 dB @ V_{ICM} = 0 V
- **Output dynamic range** up to 2 V_{pp}
- **5 V voltage supply** (Vdd = +3.5 V, Vss = -1.5 V, Vcm = 0 V)
- **Differential input impedance** 5 kΩ
- **Dif. output Impedance** 3-4 Ω

10 Current D/A Converters (5/CH)

- **8 bits**
- **FSR** two sources with 2*1.8 mA max. and 8 sources with 2*300 μA max. @ Iref = 940 μA
- **Resolution** 7 μA @ Imax = 1.8 mA; 1.2 μA @ Imax = 300 μA
- **Voltage compliance** 1 - 2 V
- **I^2C/RS485 Bus** up to 200 kHz
- **Heating current** up to 18 mA
- **Voltage supply:** Analogue components: 5 V (Vdd - Vss); Digital components: 2 V (Vdd - Vss);

Thermometer

- **Temperature range** from -30 °C to +80 °C
- **Thermometer sensitivity** up to hundreds of mV/K
- **Output signal** up to 2 V_{pp}. Output differential current drives output resistors connected to any common-mode voltage in between 3.5 V and −1.5 V (usually 0 V). Maximum dynamic range observed with 1 V common-mode voltage (*ie* middle between Vdd and Vss).
- **5 V voltage supply** (Vdd - Vss)

GENERAL DESCRIPTION

AwaXe_v3 (*Athena Warm Asic for the X-ifu Electronics - version 3*) is an upgrade ASIC developed for the Warm Front End Electronics (WFEE) of the X-IFU (X-ray Integral Field Unit) instrument in the context of the future X-ray space telescope ATHENA.

This 3^{rd} version integrates two channels of the WFEE, as shown in Figure 1. Each channel includes an ultra-low gain-drift LNA (low noise amplifier) and 5 adjustable current sources of the X-IFU readout chain. To configure the current sources, a series bus RS485/I^2C constructed by a RadHard by Design digital library addresses the 8-bit D/A converter of each current source as slow control . HK (HouseKeepig and Telemetry) elements for monitoring temperature, current and voltage are also integrated into this version. This ASIC belongs to the AwaXe and SQmux ASIC families developed at APC for the SQUID/TES readout.

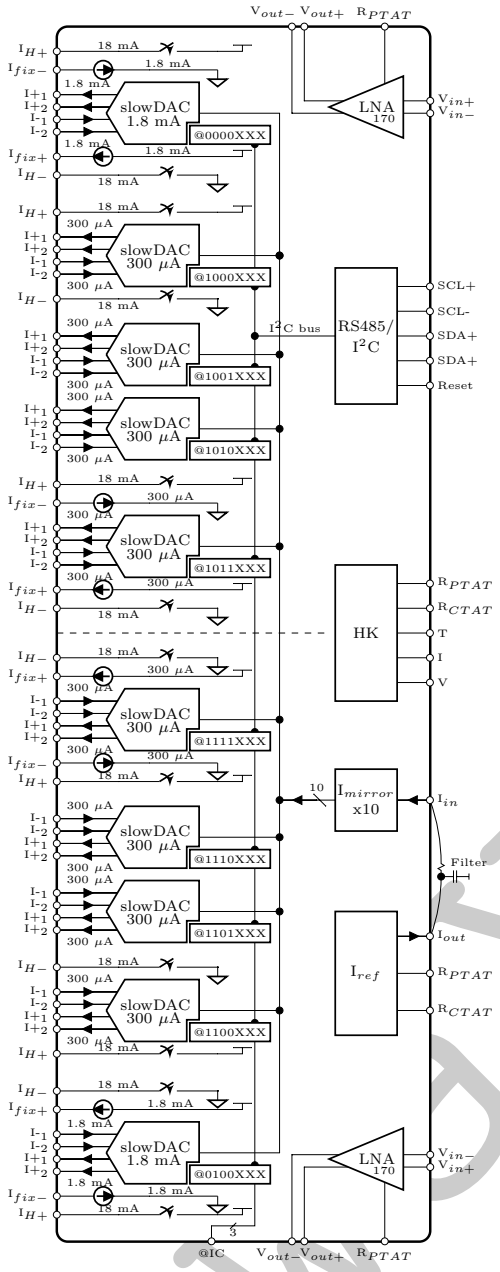

Figure 1: Block diagram of the AwaXe_v3 including two channels of the WFEE. One channel is on the top and the other is on the bottom, separated by a dash line in the middle. Each channel contains one differential low noise amplifier and 5 current DAC. Besides, the two channels share a series I^2C/RS485 bus, a current reference and HK components. addressed via a single serial bus. The on-chip I^2C bus is converted in RS485 low voltage differential signals (SCL and SDA) to communicate with outside.

SPECIFICATIONS

Power supply = 5 V for all analogue devices: Vdd = +3.5 V, Vss = −1.5 V, Vcm = 0 V (1.5 V above the lower voltage V_{ss}). For the digital series bus: Vdd = +0.5 V, Vss = −1.5 V, separated from the analogue power supply.

Nominal operating temperature = 300 K, unless otherwise noted. Tested operating temperature range : -30 °C to +80 °C

BLOCK DIAGRAM

LNA

The LNA is a fully-differential amplifier, with 2 inputs and 2 outputs (Figure 2). It equips an independent bias current, a Proportional-To-Absolute-Temperature (PTAT) current source. A resistor R_{PTAT} is needed to generate the bias current and $R_{PTAT} = 470\ \Omega$ is recommended. The current through R_{PTAT} should be about 170 μA to provide correct bias and normal functionalities. Too small bias current will lead a bad linearity and too large bias current will cause a smaller gain. Due to process gradient, R_{PTAT}'s value needed may vary from ASIC to ASIC. Before applying LNA, user should first check the bias current by measuring the voltage at the edge of R_{PTAT} (about 82 mV with 470 Ω). With this level of bias current, the LNA will consume around 40 mA, which could be another index to check LNA's operating status.

The intrinsic input impedance is basically the ratio $\frac{\beta}{g_m}$. About 5 kΩ differential input impedance is observed. In the case of input impedance matching, a feedback resistor R_{FB} can be used to connect $OUT+$ and $IN-$ and another one to connect $OUT-$ and $IN+$. This input matching is based on

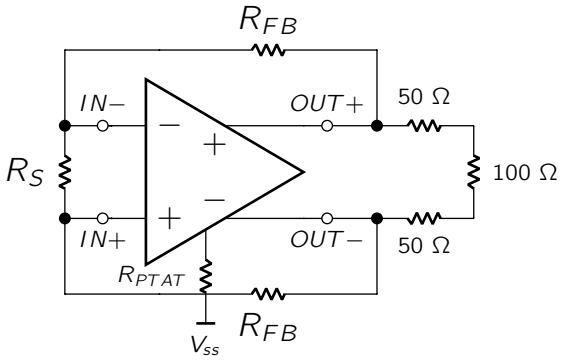

Figure 2: Simplified schematic of the LNA with external resistors basic connections. R_{PTAT} = 470 Ω was used for the characterisation.

Miller effect. Hence, the value of R_{FB} depends on the source's differential resistance R_S and the intrinsic gain of the LNA: $R_{FB} = \frac{R_S}{2} \times (Gain+1)$. In the case of $R_S = 200\ \Omega$, $R_{FB} = \frac{200}{2} \times (170+1) = 17100\ \Omega$.

The output impedance matching can be achieved by connecting two resistors at the differential output. Figure 2 illustrates a typical example with two 50 Ω at the outputs to adapt a resistive load of 100 Ω

Current source

The ASIC integrates 10 current sources and each equips an identical 8-bit DAC. Only one is shown in Figure 3. Each DAC has two identical positive ($I+_1$ and $I+_2$) outputs and two identical negative ($I-_1$ and $I-_2$) outputs. The 10 DACs share a series I^2C bus and a current reference I_{ref}, as shown in Figure 3.

To generate a current, two resistors, R_{PTAT} and R_{CTAT}, need to be connected outside the ASIC. The two resistors are indeed connected to the current reference, which combines a Proportional-To-Absolute-Temperature (PTAT) reference and a Complementary-To-Absolute-Temperature (CTAT) reference for acquiring a stable current independent to temperature.

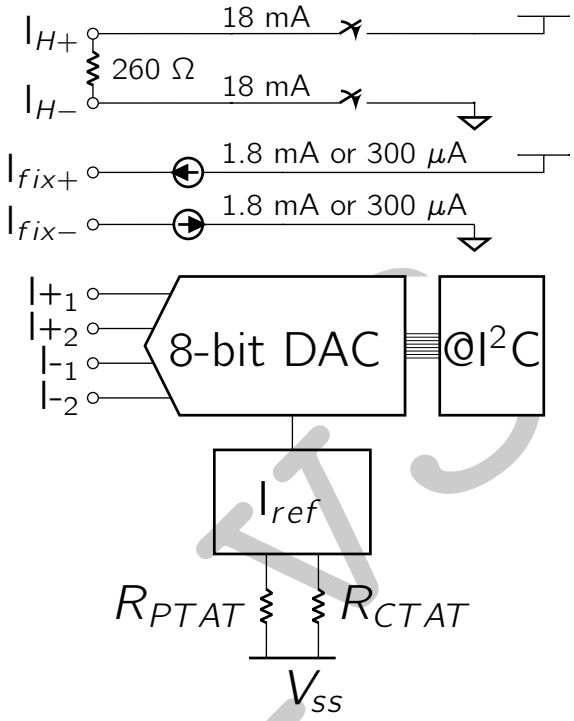

Figure 3: Simplified schematic of the current source with external resistors basic connections. Only one DAC and one I^2C decoder are shown in the diagram, representing one of the 10 pairs in the ASIC. One current reference provides an identical current to each DAC. R_{PTAT} = 342 Ω and R_{CTAT} = 6100 Ω is a used set of resistors. 2 among the 5 sources of a channel equip a pair of outputs of fixed current (I_{fix+} and I_{fix-}) equal to the maximum absolute current of a single output of DAC. 3 among the 5 sources of a channel equip a pair of outputs (I_{H+} and I_{H-}) also controlled by the I^2C bus: by connecting a 260 Ω between I_{H+} and I_{H-}, when all bits are 1, it can output a large amount of current around 18 mA; otherwise, no current will be generated.

Among the 5 current sources within a WFEE channel, one of them can provide a maximum current of 1.8 mA with a single output and for the other four, it is up to 300 μA. Furthermore, the maximum current can be still doubled by connecting a pair of outputs in the same direction.

The 8 bits allows to divide the output into

256 levels. Such configuration is realised via a series bus RS485/I^{2}C. The ASIC receives commands from an outside master coded in RS485 standard, which is differential, good to suppress common mode noise. An interface RS485/I^{2}C is used helping to convert signals to single ended, namely the I^{2}C bus inside the ASIC. Each DAC equips an attached I^{2}C decoder with different addresses, realised with a Radiation-Hardened-By-Design digital library. The decoders are configured by the bus, so that the DAC can output different levels of current.

The recommended combination of R_{PTAT} and R_{CTAT} to output current optimised around 300 K with low drift and with levels mentioned above is $R_{PTAT} = 342\ \Omega$ and $R_{CTAT} = 6100\ \Omega$. However, the process gradient may cause a drift of the optimum region where thermal fluctuation is the best compensated. In such case, it is suggested to adjust the R_{PTAT} and R_{CTAT} to have a better performance. Moreover, the output current level can also be adjusted by using different resistance.

Moreover, two auxiliary functions have been added into this ASIC. Two of the 5 current sources (see Figure 1) add a pair of fixed current output (I_{fix+} and I_{fix-}) that equals the maximum absolute current of a single output of DAC (1.8 mA or 300 μA). This function brings up two new possibilities:

- enlarge the maximum output up to 900 μA (or 5.4 mA) if users mix a I_{fix} with the two outputs of the DAC in the same direction;
- enrich the output combination. For example, by mixing a I_{fix} with the two outputs of the DAC in the opposite direction, users can have an output range of [-300 μA, 300 μA] (or [-1.8 mA, 1.8 mA]) centred at 0 and configured by 8 bits.

Another new option in this version is a pair of output (I_{H+} and I_{H-}) capable of generating a large amount of current about 18 mA if connecting a 260 Ω resistor between them. This function is also controlled by the I^{2}C bus. The control is represented as a switch in Figures 1 and 3. Only when all 8 bits are 1, the "switch" is closed and the 18 mA is generated; otherwise the "switch" is open and no current is outputted. This function can be used to heat electric conductors thanks to Joule heating. 3 of the 5 current sources have this function included, as shown in Figure 1.

Thermometer

The thermometer (Figure 4) has a pair of differential voltage outputs V_{t+} and V_{t-}. It also has independent complementary and/or proportional-to-temperature bias current. R_{CTAT} is then the resistor to adjust the complementary part of the current and R_{PTAT} the one for the current proportional to temperature. $R_{PTAT} = 300\ \Omega$ and $R_{CTAT} = 6.65\ k\Omega$ is a validated set of resistors.

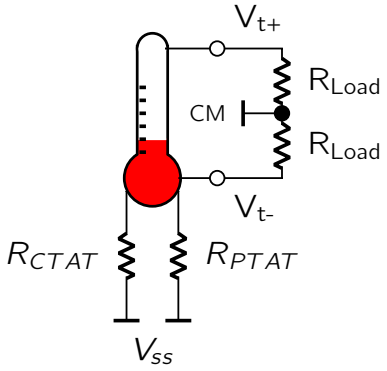

Figure 4: Simplified schematic of the thermometer with external resistors basic connections. $R_{PTAT} = 300\ \Omega$ and $R_{CTAT} = 6.65\ k\Omega$, $R_{Load} = 2.7\ k\Omega$

If 0 V output voltage is treated as a refer-

ence, the temperature corresponds to 0 V can be configured by changing a bit the R_{CTAT} resistance. For example, using a 6810 Ω resistor can refer 0 V to 22 °C, while using 6.65 $k\Omega$ sets 0 V at 27 °C.

Load resistance of 2.7 $k\Omega$ is a good trade-off in between thermometer sensitivity and wide thermal range. Using a 3.3 $k\Omega$ resistor can cause a visible non-linear response below 0 °C and above 60 °C.(refer to Figure 25).

PADs CORRESPONDANCES

This section explains the pinout of the ASIC AwaXe_v3 "bare die". The pinout are also illustrated in Figure 5.

LNA PADs DESCRIPTIONS

- vdd!_LNA_CHx (x = 1 or 2) is the "+" power supply Vdd of the LNA. Must be +3.5 V. Each LNA has an independent VDD, isolated from the other components.
- gnd!_LNA_CHx (x = 1 or 2) [1] is the "-" power supply Vss of the LNA. Must be -1.5 V [2]. The Vss of each LNA is also independent, isolated isolated from the Vss of the other components.
- R_PTAT_LNA_CHx (x = 1 or 2) must be connected to the Vss through a resistor. It is a reference resistor to generate the bias current of the "proportional to absolute temperature" current reference attached with the LNA. Typical value : R_PTAT_Ampli = 470 Ω
- In+_LNA_CHx and In-_LNA_CHx (x = 1 or 2) are the differential inputs of the LNA. They must be referred to a common mode of about 0 V.
- Out+_LNA_CHx and Out-_LNA_CHx (x = 1 or 2) are the differential outputs of the LNA. They are referred to a common mode slightly larger the 0 V (about 100 mV).

[1] gnd! is referring the minimum voltage of the ASIC corresponding to the 700 μm thick silicon substrate of the entire ASIC. Thus, this is necessarily a common reference of the different parts of the chip, for instance: LNA, DACs and Thermometer. Indeed, the Vss of these parts are not formally - ie with metal layers - connected, but a residual resistance as low as 10 Ω can be observed because of the silicon substrate conduction.

[2] A lower Vss is acceptable. In contrary, a higher Vss will reduce the maximum dynamic range of the LNA.

CURRENT SOURCE PADs DESCRIPTIONS

The current source is composed of several analogue circuits and a digital circuit. The two parts are electrically separated. The power supply pads of the two parts should not be connected together.

Analogue pads:

- "vdd!_DAC_TES_CHx", "vdd!_DAC_FEbias_CHx", "vdd!_DAC_FEfb_CHx", "vdd!_DAC_SSAfb_CHx" and "vdd!_DAC_SSAbias_CHx" (x = 1 or 2) are the "+" power supply Vdd for the DACs. Electrically, they are not connected together inside the ASIC. Each DAC has its own Vdd pad, so that they can be employed/power supplied separately. Must be **+3.5 V**
- "vdd!_Ifix_CHx" (x = 1 or 2) is the "+" power supply Vdd for the fixed current source of 1.8 mA and 300 μA. The two fixed source of one channel share one same Vdd pad, while the Vdd of two channels are electrically isolated. They are also isolated from the Vdd of the DACs inside the ASIC. Must be **+3.5 V**

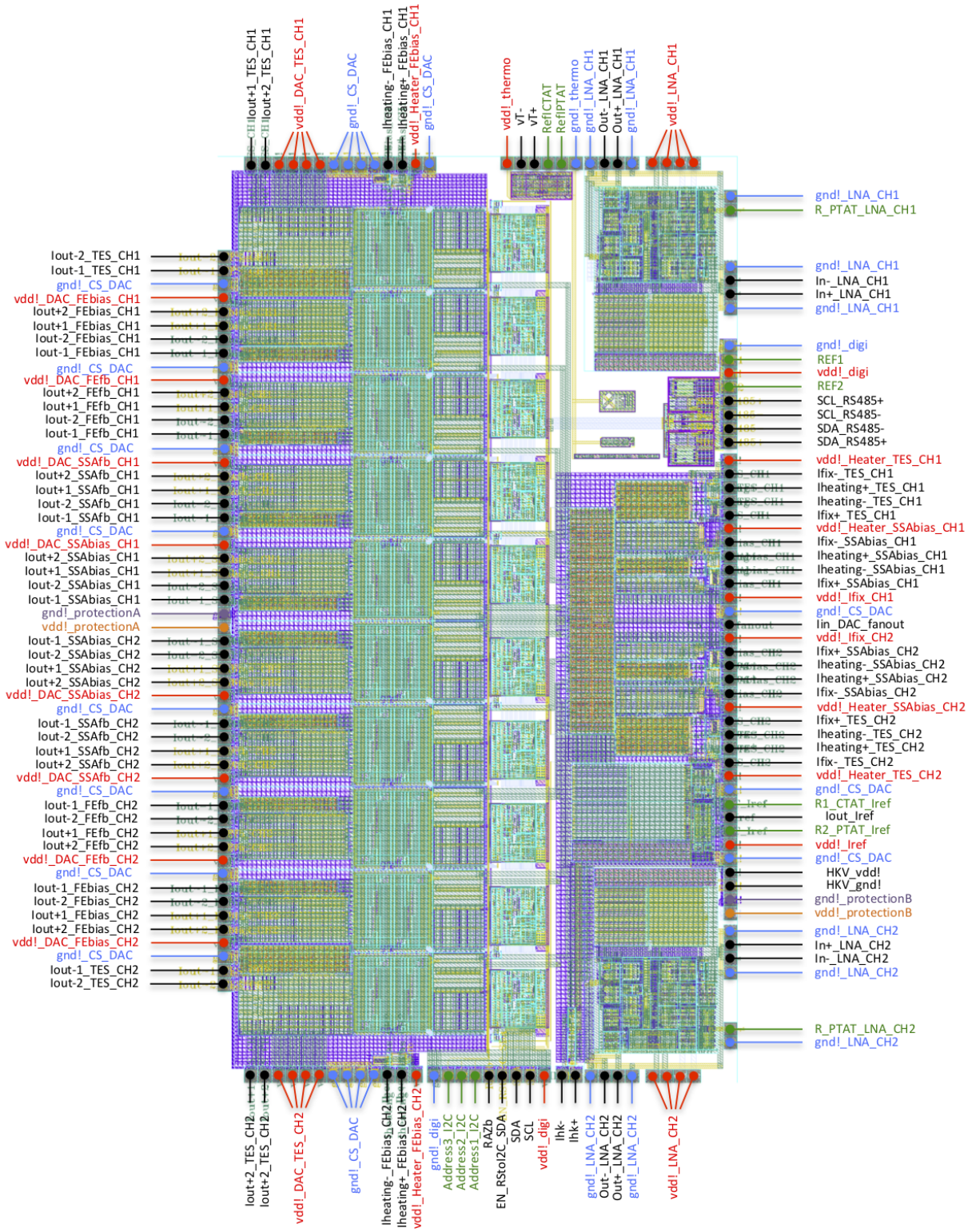

Figure 5: Microscopic photo of AwaXe_v3 at the "bare die" level. Voltage supplies +3.5 V and -1.5 V of the LNA, of the analogue circuits of the current source and of the thermometer are independent. However, they can be connected together. The dice size is about 6.75 mm x 3.79 mm. Pad pitch = 100 μm.

- "vdd!_Heater_TES_CHx", "vdd!_Heater_SSAbias_CHx" and "vdd!_Heater_FEbias_CHx" (x = 1 or 2) are the "+" power supply Vdd for the heating modules. Since these modules generate large current, each one are distributed one Vdd pad, and separated from any other Vdd pads. Must be **+3.5 V**
- "vdd!_Iref" is the "+" power supply Vdd for the current reference. Inside ASIC, it is isolated from other Vdd pads. Must be **+3.5 V**
- "gnd!_CS_DAC" is the "-" power supply Vss for all the analogue components of the current source (DACs, fixed current sources, heaters and current reference). The pads are distributed relatively evenly around the ASIC beside different devices. These pads are all connected together via metal layers inside the ASIC. For the same reason as for the LNA, they must be **-1.5 V**.
- "R1_CTAT_Iref" must be connected to the Vss through a resistor. It is a reference resistor to generate current "complementary proportional to absolute temperature". **6100** Ω typical value.
- "R2_PTAT_Iref" must be connected to the Vss through a resistor. It is a reference resistor to generate current "proportional to absolute temperature" current reference. **342** Ω typical value.
- "Iout_Iref" is the output of the current reference, about 940 μA with the recommended reference resistors. It must be connected to the pad "Iin_DAC_fanout", so that the DACs and the fixed current sources can be biased.
- "Iin_DAC_fanout" is the current input of an NMOS current mirror inside the ASIC to bias all the DACs and fixed current sources. It needs to be connected to "Iout_Iref" to get the reference current, otherwise the components will not work. Such arrangement allows to measure directly the reference current, to verify its function. Another advantage is that it is possible to connect a large-value low-pass capacitor on PCB, helping to filter the noises from the reference. Using a 100 μF allows to filter noises below 100 Hz considering about a hundred ohms of the output impedance ($\frac{1}{g_m}$) of the connected MOS transistor inside the ASIC.
- "Iout-n_TES_CHx", "Iout-n_FEbias_CHx", "Iout-n_FEfb_CHx", "Iout-n_SSAfb_CHx" and "Iout-n_SSAbias_CHx" (x = 1 or 2, n=1 or 2) are the outputs of the DAC that provide negative current. Iout-1 and Iout-2 are identical and can be connected together to double the current.
- "Iout+n_TES_CHx", "Iout+n_FEbias_CHx", "Iout+n_FEfb_CHx", "Iout+n_SSAfb_CHx" and "Iout+n_SSAbias_CHx" (x = 1 or 2, n=1 or 2) are the outputs of the DAC that provide positive current. Iout+1 and Iout+2 are identical and can be connected together to double the current. The current source of this version is differential, capable of providing at the same time negative and positive current, different from the version in ASIC AwaXe_v2.5.
- "Ifix+_TES_CHx", "Ifix-_TES_CHx", "Ifix+_SSAbias_CHx" and "Ifix-_SSAbias_CHx" (x = 1 or 2) are

the outputs of the fixed current sources. "Ifix+_TES_CHx" and "Ifix-_TES_CHx" are the differential pair of 1.8 mA. "Ifix+_SSAbias_CHx" and "Ifix-_SSAbias_CHx" are the differential output of 300 μA.

- "Iheating+_TES_CHx" and "Iheating-_TES_CHx", "Iheating+_SSAbias_CHx" and "Iheating-_SSAbias_CHx", and "Iheating+_FEbias_CHx" and "Iheating-_FEbias_CHx" (x = 1 or 2) are three pairs of differential outputs to generate a large current as a heating function. Connecting a 260 Ω resistor between a pair of outputs can obtain about 18 mA.

Digital pads:

- "vdd!_digi" is the "+" power supply Vdd for the digital circuits of the current source. Must be **+0.5 V**. Must be isolated from the analogue parts. A simple 680 Ω resistance in series with the analog VDD (+3.5 V) allows to drop the voltage to the +0.5 V. Indeed, about 5 mA is required for the digital part, mainly for the 2 RS485 drivers. Otherwise, another regulator is required to provide 2 V referring the minimum voltage.
- "gnd!_digi" is the "-" power supply Vss for the digital circuits of the current source. Must be **-1.5 V**. Must use another power supply different from the -1.5 V for the analogue parts. Must be isolated from the analogue parts.
- "REF1" and "REF2" need to be respectively connected to Vss through a resistor. They are used to transform the I^2C SDA and SCL signals between differential and single-end. **2.7 k**Ω typical value.
- "SDA_RS485+" and "SDA_RS485-" are the differential data lines using I^2C protocol and respecting for the RS485 standard.
- "SCL_RS485+" and "SCL_RS485-" are the differential clock lines using I^2C protocol and respecting for the RS485 standard.
- "RAZb" is to reset the values in the registers within the digital circuits to zero. Must be Vss in operation, and vdd!_digi one time in the beginning.
- "Address1_I2C", "Address2_I2C" and "Address3_I2C" are the last three LSB of I^2C decoders' address. They can be consequently configured outside the ASIC, to differentiate the DACs within different ASICs but mounted on the same PCB or even on different PCBs but in the same box.
- "SDA" is the single-ended data line using I^2C protocol to configure all the DACs.
- "SCL" is the single-ended clock line using I^2C protocol for all the DACs.
- "EN_RStoI2C_SDA" is used to configure the read/write direction: "1" is for the external module to write on the bus to I^2C decoders and "0" is for the external module to read from I^2C decoders.

THERMOMETER PADs DESCRIPTIONS

- vdd!_thermo is the "+" power supply Vdd of the thermometer. Must be +3.5 V[3].
- gnd!_thermo is the "-" power supply Vss of the thermometer. Must be -1.5 V[4].

[3] Referring to the LNA
[4] Referring to the LNA

- RefICTAT must be connected to the Vss through a resistor. It is a reference resistor which allows to fix the "complementary proportional to absolute temperature" current reference. Typical value 300 Ω.

- RefIPTAT must be connected to the Vss through a resistor. It is a reference resistor which allows to fix the "proportional to absolute temperature" current reference. Typical value 6800 Ω.

- vT+ and vT- are the differential outputs of the thermometer. They are in fact a pair of differential current outputs which must be loaded by resistors (R_{Load}, see Figure 4) referred to any common mode in the range [Vss-Vdd]. R_{Load} resistors can be placed very (1) near the chip or (2) near the equipment used to measured the Vt. Both solutions work. The first one allows to minimise the effect of the temperature sensitivity of the load resistors itself, because they roughly follow the ASIC temperatures. The second solutions allows to minimise the common mode coupling because of the very high output impedance of these thermometer outputs consequently only referred to voltage to the measurement equipment.

Other PADs DESCRIPTIONS

- "Ihk+" and "Ihk-" is a pair of differential current output to monitor the current reference. The current should be about 240 μA.

- "HKV_vdd!" and "HKV_gnd!" are two pads to monitor the power supply Vdd (+3.5 V) and Vss (-1.5 V) of the current reference.

- "vdd!_protectionA", "gnd!_protectionA", "vdd!_protectionB" and "gnd!_protectionB" are the pads for the other pads' protection. "A" or "B" represent different protection region. In other words, each only protects a part of the ASIC. Hence, it is necessary to connect all the pads for a full protection[5].

PACKAGE DESCRIPTION

The ASIC AwaXe_v3 can either be provided as a bare-die (Figure to be added) or packaged in **CQFP208** (Figure to be added). The bonding diagram of the packaging is shown in Figure 6, following Table 1 listing the pinout. The pins names are kept the same as the bare-die level. Users can refer to the section "PADs CORRESPONDANCES" for the descriptions in case of needs.

PIN FUNCTIONS

Table 1: CQFP208 Pinout

No.	Name	Part
1	gnd!_CS_DAC	All 10 Current sources
2	Iout-1_TES_CH2	Current source - DAC 0100XXX
3	Iout-2_TES_CH2	Current source - DAC 0100XXX
4	Iout+1_TES_CH2	Current source - DAC 0100XXX
5	Iout+2_TES_CH2	Current source - DAC 0100XXX
6	vdd!_DAC_TES_CH2	Current source - DAC 0100XXX
7	vdd!_DAC_TES_CH2	Current source - DAC 0100XXX
8	vdd!_DAC_TES_CH2	Current source - DAC 0100XXX
9	vdd!_DAC_TES_CH2	Current source - DAC 0100XXX
10	gnd!_CS_DAC	All 10 Current sources
11	gnd!_CS_DAC	All 10 Current sources
12,13	nc	
14	gnd!_CS_DAC	All 10 Current sources
15	gnd!_CS_DAC	All 10 Current sources
16	Iheating-_FEbias_CH2	Current source - Heater - DAC 1100XXX
17	Iheating+_FEbias_CH2	Current source - Heater - DAC 1100XXX
18	vdd!_Heater_FEbias_CH2	Current source - Heater - DAC 1100XXX
19,20	nc	
21	gnd!_digi	Current source - I^2C bus
22	Address3_I2C	Current source - I^2C bus
23	Address2_I2C	Current source - I^2C bus
24	Address1_I2C	Current source - I^2C bus
25	RAZb	Current source - I^2C bus
26	EN_RStoI2C_SDA	Current source - I^2C bus
27	SDA	Current source - I^2C bus
28	SCL	Current source - I^2C bus
29	vdd!_digi	Current source - I^2C bus
30,31	nc	
32	Ihk-	Current HK module
33	Ihk+	Current HK module
34,35	nc	
36	gnd!_LNA_CH2	LNA channel 2

[5]Except for the two LNA, who do not integrate pads protection.

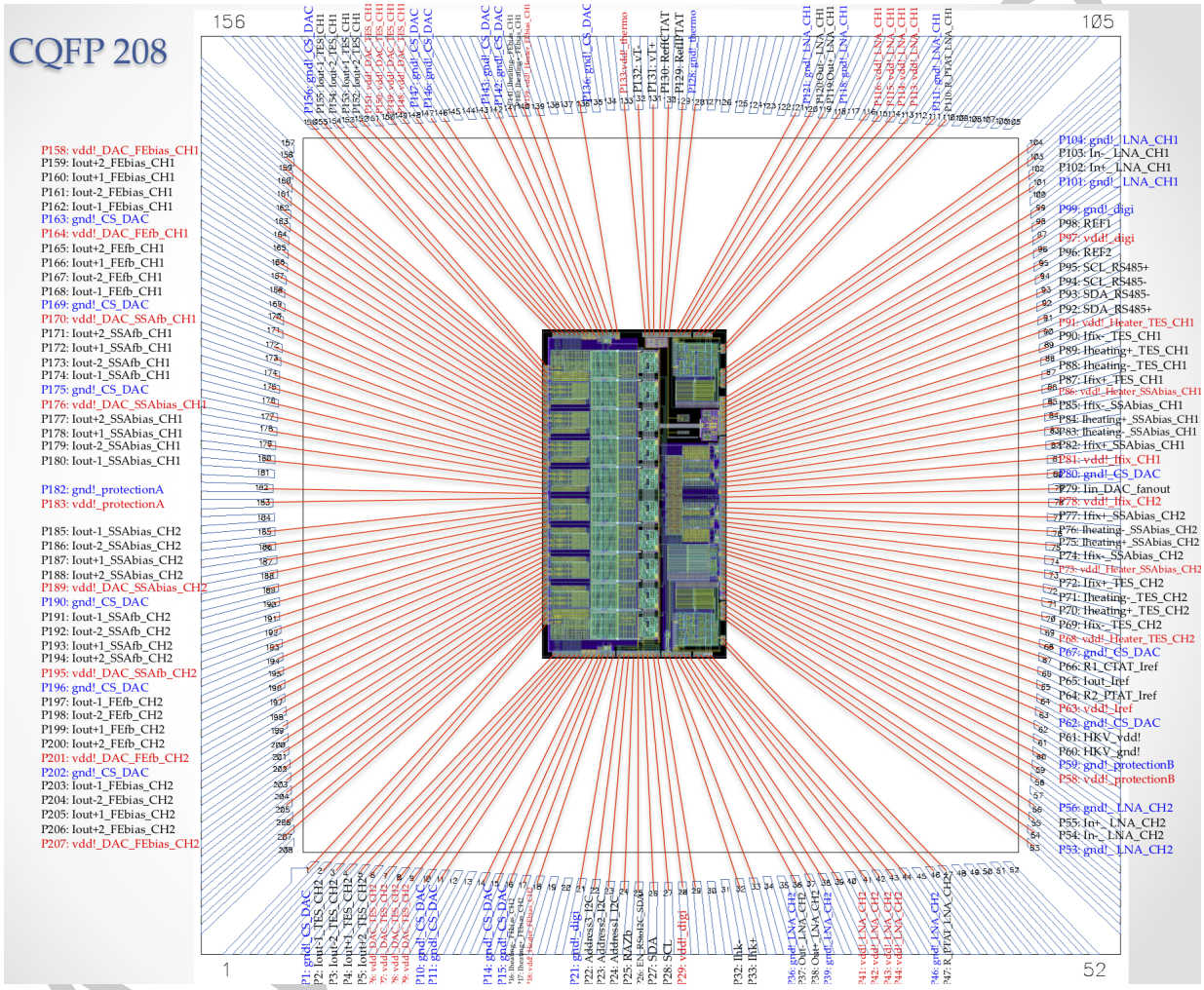

Figure 6: CQFP 208 bonding diagram and Pin connections. Pin 1 and 207 are on the bottom left. Not connected pins can be left open or connected to Vss (preferred for thermal and EMC reasons)

37	Out-_LNA_CH2	LNA channel 2
38	Out+_LNA_CH2	LNA channel 2
39	gnd!_LNA_CH2	LNA channel 2
40	nc	
41	vdd!_LNA_CH2	LNA channel 2
42	vdd!_LNA_CH2	LNA channel 2
43	vdd!_LNA_CH2	LNA channel 2
44	vdd!_LNA_CH2	LNA channel 2
45	nc	
46	gnd!_LNA_CH2	LNA channel 2
47	R_PTAT_LNA_CH2	LNA channel 2
48-52	nc	
53	gnd!_LNA_CH2	LNA channel 2
54	In-_LNA_CH2	LNA channel 2
55	In+_LNA_CH2	LNA channel 2
56	gnd!_LNA_CH2	LNA channel 2
57	nc	
58	vdd!_protectionB	Pads
59	gnd!_protectionB	Pads
60	HKV_gnd!	Voltage HK function
61	HKV_vdd!	Voltage HK function
62	gnd!_CS_DAC	All 10 Current sources
63	vdd!_Iref	Current source - I_{ref}
64	R2_PTAT_Iref	Current source - I_{ref}
65	Iout_Iref	Current source - I_{ref}
66	R1_CTAT_Iref	Current source - I_{ref}
67	gnd!_CS_DAC	All 10 Current sources
68	vdd!_Heater_TES_CH2	Current source - Heater - DAC 0100XXX
69	Ifix-_TES_CH2	Current source - I_{fix}
70	Iheating+_TES_CH2	Current source - Heater - DAC 0100XXX
71	Iheating-_TES_CH2	Current source - Heater - DAC 0100XXX
72	Ifix+_TES_CH2	Current source - I_{fix}
73	vdd!_Heater_SSAbias_CH2	Current source - Heater - DAC 1111XXX
74	Ifix-_SSAbias_CH2	Current source - I_{fix}
75	Iheating+_SSAbias_CH2	Current source - Heater - DAC 1111XXX
76	Iheating-_SSAbias_CH2	Current source - Heater - DAC 1111XXX
77	Ifix+_SSAbias_CH2	Current source - I_{fix}
78	vdd!_Ifix_CH2	Current source - Both I_{fix} in channel 2
79	Iin_DAC_fanout	All 10 Current sources
80	gnd!_CS_DAC	All 10 Current sources
81	vdd!_Ifix_CH1	Current source - Both I_{fix} in channel 1
82	Ifix+_SSAbias_CH1	Current source - I_{fix}
83	Iheating-_SSAbias_CH1	Current source - Heater - DAC 1011XXX
84	Iheating+_SSAbias_CH1	Current source - Heater - DAC 1011XXX
85	Ifix-_SSAbias_CH1	Current source - I_{fix}
86	vdd!_Heater_SSAbias_CH1	Current source - Heater - DAC 1011XXX
87	Ifix+_TES_CH1	Current source - I_{fix}
88	Iheating-_TES_CH1	Current source - Heater - DAC 0000XXX
89	Iheating+_TES_CH1	Current source - Heater - DAC 0000XXX
90	Ifix-_TES_CH1	Current source - I_{fix}
91	vdd!_Heater_TES_CH1	Current source - Heater - DAC 0000XXX
92	SDA_RS485+	Current source - I^2C bus
93	SDA_RS485-	Current source - I^2C bus
94	SCL_RS485-	Current source - I^2C bus
95	SCL_RS485+	Current source - I^2C bus
96	REF2	Current source - I^2C bus
97	vdd!_digi	Current source - I^2C bus
98	REF1	Current source - I^2C bus
99	gnd!_digi	Current source - I^2C bus
100	nc	
101	gnd!_LNA_CH1	LNA channel 1
102	In+_LNA_CH1	LNA channel 1
103	In-_LNA_CH1	LNA channel 1
104	gnd!_LNA_CH1	LNA channel 1
105-109	nc	
110	R_PTAT_LNA_CH1	LNA channel 1
111	gnd!_LNA_CH1	LNA channel 1
112	nc	
113	vdd!_LNA_CH1	LNA channel 1
114	vdd!_LNA_CH1	LNA channel 1
115	vdd!_LNA_CH1	LNA channel 1
116	vdd!_LNA_CH1	LNA channel 1
117	nc	
118	gnd!_LNA_CH1	LNA channel 1
119	Out+_LNA_CH1	LNA channel 1
120	Out-_LNA_CH1	LNA channel 1
121	gnd!_LNA_CH1	LNA channel 1
122-127	nc	
128	gnd!_thermo	HK - thermometer
129	RefIPTAT	HK - thermometer
130	RefICTAT	HK - thermometer
131	VT+	HK - thermometer
132	VT-	HK - thermometer
133	vdd!_thermo	HK - thermometer
134-135	nc	
136	gnd!_CS_DAC	All 10 Current sources
137-138	nc	
139	vdd!_Heater_FEbias_CH1	Current source - Heater - DAC 1000XXX
140	Iheating+_FEbias_CH1	Current source - Heater - DAC 1000XXX
141	Iheating-_FEbias_CH1	Current source - Heater - DAC 1000XXX
142	gnd!_CS_DAC	All 10 Current sources
143	gnd!_CS_DAC	All 10 Current sources
144-145	nc	
146	gnd!_CS_DAC	All 10 Current sources
147	gnd!_CS_DAC	All 10 Current sources
148	vdd!_DAC_TES_CH1	Current source - DAC 0000XXX
149	vdd!_DAC_TES_CH1	Current source - DAC 0000XXX
150	vdd!_DAC_TES_CH1	Current source - DAC 0000XXX
151	vdd!_DAC_TES_CH1	Current source - DAC 0000XXX
152	Iout+2_TES_CH1	Current source - DAC 0000XXX
153	Iout+1_TES_CH1	Current source - DAC 0000XXX
154	Iout-2_TES_CH1	Current source - DAC 0000XXX
155	Iout-1_TES_CH1	Current source - DAC 0000XXX
156	gnd!_CS_DAC	All 10 Current sources
157	nc	
158	vdd!_DAC_FEbias_CH1	Current source - DAC 1000XXX
159	Iout+2_FEbias_CH1	Current source - DAC 1000XXX
160	Iout+1_FEbias_CH1	Current source - DAC 1000XXX
161	Iout-2_FEbias_CH1	Current source - DAC 1000XXX
162	Iout-1_FEbias_CH1	Current source - DAC 1000XXX
163	gnd!_CS_DAC	All 10 Current sources
164	vdd!_DAC_FEfb_CH1	Current source - DAC 1001XXX
165	Iout+2_FEfb_CH1	Current source - DAC 1001XXX
166	Iout+1_FEfb_CH1	Current source - DAC 1001XXX
167	Iout-2_FEfb_CH1	Current source - DAC 1001XXX
168	Iout-1_FEfb_CH1	Current source - DAC 1001XXX
169	gnd!_CS_DAC	All 10 Current sources
170	vdd!_DAC_SSAfb_CH1	Current source - DAC 1010XXX
171	Iout+2_SSAfb_CH1	Current source - DAC 1010XXX
172	Iout+1_SSAfb_CH1	Current source - DAC 1010XXX
173	Iout-2_SSAfb_CH1	Current source - DAC 1010XXX
174	Iout-1_SSAfb_CH1	Current source - DAC 1010XXX
175	gnd!_CS_DAC	All 10 Current sources
176	vdd!_DAC_SSAbias_CH1	Current source - DAC 1011XXX
177	Iout+2_SSAbias_CH1	Current source - DAC 1011XXX
178	Iout+1_SSAbias_CH1	Current source - DAC 1011XXX
179	Iout-2_SSAbias_CH1	Current source - DAC 1011XXX
180	Iout-1_SSAbias_CH1	Current source - DAC 1011XXX
181	nc	
182	gnd!_protectionA	Pads
183	vdd!_protectionA	Pads
184	nc	
185	Iout-1_SSAbias_CH2	Current source - DAC 1111XXX
186	Iout-2_SSAbias_CH2	Current source - DAC 1111XXX
187	Iout+1_SSAbias_CH2	Current source - DAC 1111XXX
188	Iout+2_SSAbias_CH2	Current source - DAC 1111XXX
189	vdd!_DAC_SSAbias_CH2	Current source - DAC 1111XXX
190	gnd!_CS_DAC	All 10 Current sources
191	Iout-1_SSAfb_CH2	Current source - DAC 1110XXX
192	Iout-2_SSAfb_CH2	Current source - DAC 1110XXX
193	Iout+1_SSAfb_CH2	Current source - DAC 1110XXX
194	Iout+2_SSAfb_CH2	Current source - DAC 1110XXX
195	vdd!_DAC_SSAfb_CH2	Current source - DAC 1110XXX
196	gnd!_CS_DAC	All 10 Current sources
197	Iout-1_FEfb_CH2	Current source - DAC 1101XXX
198	Iout-2_FEfb_CH2	Current source - DAC 1101XXX
199	Iout+1_FEfb_CH2	Current source - DAC 1101XXX
200	Iout+2_FEfb_CH2	Current source - DAC 1101XXX
201	vdd!_DAC_FEfb_CH2	Current source - DAC 1101XXX
202	gnd!_CS_DAC	All 10 Current sources
203	Iout-1_FEbias_CH2	Current source - DAC 1100XXX
204	Iout-2_FEbias_CH2	Current source - DAC 1100XXX
205	Iout+1_FEbias_CH2	Current source - DAC 1100XXX
206	Iout+2_FEbias_CH2	Current source - DAC 1100XXX
207	vdd!_DAC_FEbias_CH2	Current source - DAC 1100XXX
208	nc	

APPLICATION - TYPICAL USE

Analogue power supply

The LNAs, the current sources and the thermometer must respect the following two bias conditions to function correctly:

- Vdd - Vss = 5 V
- Vcm - Vss = 1.5 V

Vcm is the bias voltage needed for the base of the front-end bipolar transistors, thus referred the **common mode** of the differential input signal. For a typical current gain β about 200 A/A, the expected

base current supplied by the Vcm is therefore 200 times smaller than the input stage collector current ($\approx$ 2 mA). Regarding the small curent $2 \times \frac{I_C}{\beta} \approx 20\ \mu A$, the Vcm can be generated by a voltage reference. Indeed, in addition to the base current of the LNA input stage, slow DAC possibly has a small difference between the differential outputs, that can also create a small current of several micro-amps circulating in this same common mode voltage. So a voltage reference allows keeping constant the common mode voltage referring to the lower voltage (Vss=gnd!). A voltage reference of 1.5 V, "ISL21080", has been successfully used with the schematic shown in Figure 7. The device data-sheet proposed to add a "noise reduction network" based on a 2 kΩ resistor in series with a 10 μF capacitor in parallel with the Vcm (not represented in this document).

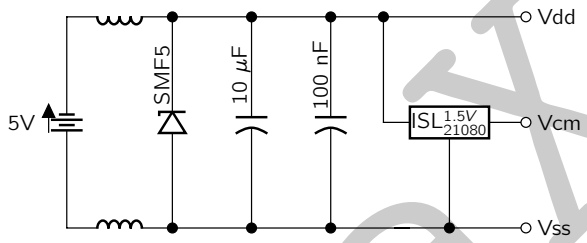

Figure 7: Proposed schematic to provide the Vcm=1.5 V from a single 5 V (Vdd - Vss) power supply using an "ISL21080" 1.5 V voltage reference.

A diode is also recommended to prevent ESD discharge, over-voltage, spike and/or inversion during power supply connections. Devices as "SMF5V0A" or "DO-214BA GF1D" can be used. Only the first one prevents over-voltage.

Digital power supply

The digital series bus must respect the following two conditions to function correctly:

- Vdd - Vss = 2 V
- Vcm - Vss = 1.5 V

The power supply for the digital parts should be isolated from the analogue supply.

Power supply decoupling philosophy

LNA, Slow DAC and thermometer have their own power supplies Vdd, Vcm and Vss. To prevent any disturbance from one system to the other, each device should equip a dedicated capacitor bank. Although a very large capacitance can theoretically filter down to very low frequency, parasitic resistances and inductances will degrade the filtering effect at higher frequency range. Hence, 3 capacitors respectively in the order of a few μF, 100 nF and 1 nF are recommended to be used in parallel. Assuming that a larger capacitance causes a larger equivalent series resistance (ESR), it is better to place the smallest capacitors as close as possible to the chips.

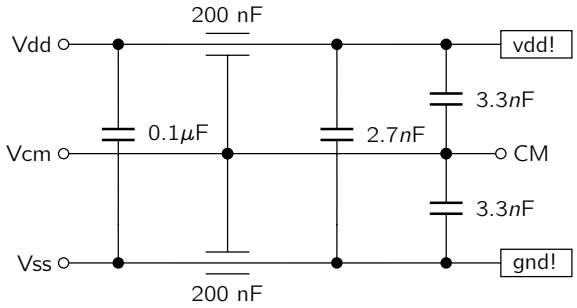

Figure 8: Proposed power supply filtering using a bank of 3 capacitors between every two voltages. 22 μF or 10 μF MLCC X5R or Tantal 10 V + 100 nF 100 V COG. or 200 nF 50 V three terminal capacitors NFM41p + 2.7 or 3.3 nF 25 V MLCC COG.

Typical use of the series bus RS485/I^{2}C

RS485 is a standard that defines the electrical behaviours between drivers and receivers on the physical level, but does not concern the protocol to be used. In the case of "AwaXe" series ASICs, the internal bus uses only single-ended I^{2}C protocol and the external communication uses I^{2}C protocol applying RS485 standard.

RS485 standard

The standard defines a type of differential communication, notably helpful to improve the common-mode rejection. As shown in Figure 9, signals are transmitted via a pair of differential lines. The two lines need a potential difference of at least 200 mV. If line A is 200 mV higher than line B, then output shows high level; If line A is 200 mV lower than line B, then output shows low level. When the bus is idle, the potential difference of 200 mV is always present. The bus cannot work with a potential difference below 200 mV, in which case the output cannot be well defined.

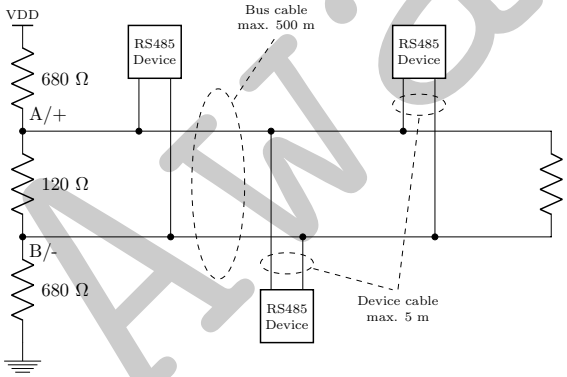

Figure 9: RS485 bus.

Except the pull-up and pull-down resistors (e.g. 680 Ω in Figure 9), termination resistors typically of 120 Ω are also needed at both ends of the two differential lines, to reduce the signal reflection.

I^{2}C protocol

The protocol proposes two lines for data communication. As shown in Figure 10, one is "SDA" as the data line, and the other is "SCL" as the clock line. The protocol is not differential but can adapt easily to RS485 standard. The device that generates the clock is the master. Both two lines are connected to Vdd via a resistor of several kilo ohm, to lift the lines to high level.

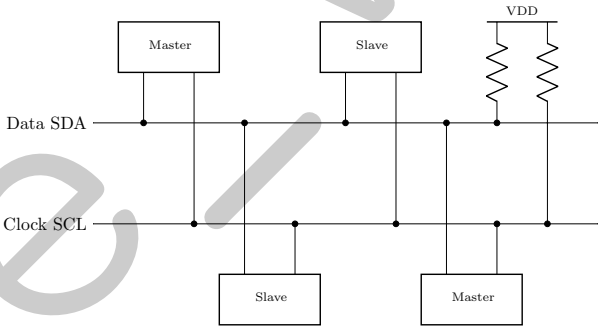

Figure 10: I^{2}C Wiring

The timing diagram of Figure 11 illustrates the principle of I^{2}C communication. When the bus is idle, both line stay at high level. When the SCL line is at high level, a falling edge of the SDA line represents a START of the communication. An address of 7-bit is first written by the master on the bus, followed by the 8th bit showing the direction of data transfer. The slave of the correct address will then write one bit as acknowledgement. After the confirmation, the data transfer starts, each time sending 8-bit data, followed by 1-bit of acknowledgement from the slave. The communication ends when SDA has a rising edge and at the same time SCL is at high level, as the STOP condition.

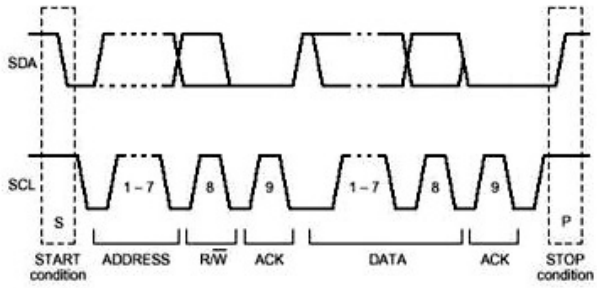

Figure 11: I²C timing diagram

Series bus in the ASIC AwaXe_v3

Ten I²C decoders are integrated in the ASIC AwaXe_v3. They all act as slaves, but can either read from or write on the bus. Each decoder has a different address of 7 bits, $b_6b_5b_4b_3b_2b_1b_0$:

- b_6 the MSB differentiates the current sources with different output levels 1.8 mA and 300 μA: b_6=0 for the sources of 1.8 mA and b_6=1 for the ones of 300 μA;
- b_5 is used to differentiate the two channels within one ASIC: b_5=0, channel 1; b_5=1, channel 2.
- b_4b_3 are used to differentiate the 4 sources of 300 μA of the same channel;
- $b_2b_1b_0$ are left to differentiate the decoders within different packagings on the same bus.

$b_6b_5b_4b_3$ are fixed inside the ASIC while $b_2b_1b_0$ are not. These last three bits have their own pads, thus they can be configured outside the ASIC.

The 8th bit is kept to indicate to read or write. The master writes data to the slave when it is 0 and reads from the slave when it is 1. The SCL line can support up to 400 kHz. Both the SCL line and the SDA line in the ASIC are single-ended. However, an interface RS485/I²C is equipped to transfer the single-ended lines to differential lines applying RS485 standard.

PCB - Evaluation boards

The evaluation boards (Figures to be added) are still being developed. However, the design principles stay the same as the ones for "AwaXe_v2" and "AwaXe_v2.5", which will be described in this section.

Using 5 V power supply, the analogue circuits need a voltage regulator "ISL21080" to generate its common mode voltage 1.5 V, and the digital parts need a voltage regulator "STLQ015M20R" or "LP2985AIM5-2.0/NOPB" to generate the 2 V digital Vdd.

After the regulators, EMI filter capacitors (200 nF "NFM41p", as shown in Figure 8) ensures the connection between the power supply of a part of the circuit and the supply planes Vdd, Vss and Vcm of the PCB.

The differential LNA has common-mode filters (CMF: "ACP3225-102-2P-T000") directly connected at its input and the output. It improves the common-mode noise rejection and the symmetry of the signals.

6.8 V or 9.1 V zener diodes ("TVS" 6.8 V or 9.1 V "SOT23") protect the differential input and output of any overvoltages (ESD suppressor). Such diodes should also be used between the differential digital lines: between "SDA_RS485-" and "SDA_RS485+", and between "SCL_RS485-" and "SCL_RS485+".

The common mode input bias of the LNA uses two 10 kΩ resistors connected to Gnd (0 V). With $I_b = \frac{I_C}{\beta} \approx 10$ μA, the voltage drop of about 100 mV can be considered negligible at the input of the LNA. The noise contribution of about 10 nV/$\sqrt{Hz}$ of these 10 kΩ resistors is strongly attenuated by the

voltage bridge divider formed by the 10 kΩ itself and the source impedance: Assuming 200 Ω source resistance, the 10 $nV/\sqrt{Hz}$ Johnson noise contribution is finally reduced by about two order of magnitude, meaning about 100 $pV/\sqrt{Hz}$ which is significantly less than the LNA intrinsic noise.

Input matching is achieved using feedback resistors R_{FB}. The input impedance of open loop is about 5 kΩ. R_{FB} emulates a Miller input impedance of about $R_{FB}/170$. To adapt 200 Ω source resistance, ≈17100 Ω feedback resistors R_{FB} should be used.

The LNA intrinsic differential output impedance equals about 4 Ω ($2k_BT/qIc$). The output matching is obtained by adding extra 47-50 Ω resistors in series with outputs, to adapt 100 Ω load.

A typical 470 Ω R_{PTAT} resistor is used to generate bias current. The current is proportional to absolute temperature, allowing to minimise gain drift (compensating the decrease of the transconductance with temperature). However, the value of R_{PTAT} needs to be verified by measuring the voltage at the edge of R_{PTAT}, that needs to be about 82 mV, before operating the LNA.

ESD CAUTION

ASICs are ESD (Electro-Static Discharge) sensitive devices. Human body and test equipment readily accumulate electrostatic charges as high as few kV that may discharge without detection. Although many protections exist in the chip and on the proposed evaluation board, proper ESD precautions should be taken to avoid performance degradations, loss of functionalities or any other damage which may occur on devices subjected to high energy ESD.

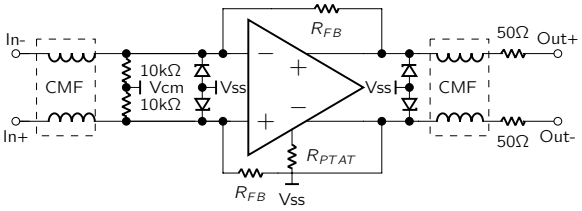

Figure 12: Schematic showing the discret devices implemented on the evaluation board to operate the LNA. Common-mode filters (CMF: ACP3225-102-2P-T000) to improve symmetry and to reject common-mode noise; ESD suppressor diodes (TVS 9.1 V or 6.8 V SOT23) at the input and the output avoiding any over-voltages; 10 kΩ resistors to bias the bases of the input transistors ($I_b \approx 10\ \mu A$); Feedback resistors R_{FB} ≈17100 Ω to acheive input matching; 50 Ω resistors to match a 100 Ω line at the output; A typical 470 Ω resistor R_{PTAT} is used to generate bias current and helps to minimise gain drift.

TYPICAL PERFORMANCES

LNA

The ASIC AwaXe_v3 adopts exactly the same LNA as the one integrated into the ASIC AwaXe_v2.5. Considering the fact that the LNAs in the past ASICs (AwaXe_v2 and AwaXe_v2.5) have very coherent measurement results, this part for now keeps using the measurement of v2.5. The main measured performances are first resumed in Table 2.

Table 2: LNA performance

Parameter	Conditions	Typ	Unit
Gain	DC-10 MHz	170	V/V
BW	-1 dB	17.5	MHz
e_n	white	<1	$nV/\sqrt{Hz}$
i_n	white	<3	$pA/\sqrt{Hz}$
Corner Frequency	1/f	<4	kHz
Non-linearity	on 1 $V_{diff-out_{pp}}$	<1%	
Gain drift	11-75 °C	<350	ppm/K
Consumption		190	mW

Differential voltage gain

Figure 13 gives gain, noise and phase measurements compared to simulations. In practice, the measured loaded gain equals about 85 V/V. The measured bandwidth of a full wired LNA is around 17.5 MHz including 2 m cables for connections to the input and the output of the LNA. The bottom curves of Figure 13 show the phase shift of about 16.6° at 5 MHz[6] at the output of the LNA.

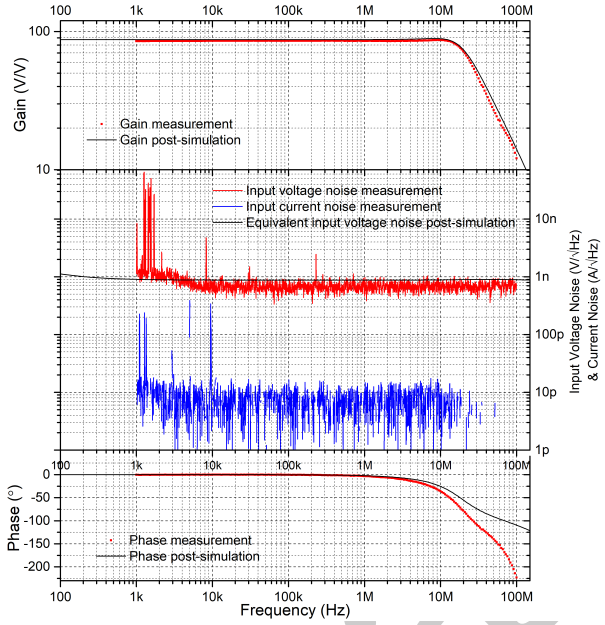

Figure 13: (top) Measured and simulated loaded gain ; (middle) equivalent input noise, voltage in blue and current in red; (bottom) phase of the LNA at room temperature *ie* 300 K.

Equivalent input noises

The noise of the amplifier illustrated in the middle of Figure 13 is characterised by input voltage e_n and current noises i_n. The total input voltage noise density $\sqrt{S_v}$ is the contribution of both input noise, where the current noise contribution is via the differential impedance of the source R_S. The main noise contributors include the input and output shot noise of the front-end bipolar transistors, thermal voltage noise from the parasitic access resistance of the base of the front-end bipolar transistors and the noises generated by the following two stages of the LNA.

The measured and simulated equivalent input voltage noise are shown in Figure 13, where both are below 1 nV/$\sqrt{Hz}$ @ f > 1 kHz.

The simulation result is slightly larger than the measured voltage noise. It is because the simulated noise is the equivalent input noise, including the current noise contribution through the source impedance $i_n R_S$. On the other hand, the measurement of the voltage noise was performed with input short-circuited, thus excluding the current noise. The current noise has to be measured separately, because the thermal noise generated by the resistor used for the current noise measurement is larger than 1 $nV/\sqrt{Hz}$, and the voltage noise of the LNA will be overwhelmed by this thermal noise term and cannot be precisely measured.

Input impedance matching

Figure 14 compares several parameters with (close loop) and without (open loop) input matching: the gain, input voltage, out voltage and input impedance. The gain on the top was always measured at the direct input of the LNA with output loaded, which is the reason that it equals about 80 V/V but not 40 V/V. The input impedance on the bottom is differential, with about 5 kΩ without matching and about 100 Ω with the resistive feedback to match two 50 Ω as source

[6] The phase measurement does not concern the LNA's own stability, but could be useful if the LNA is used in a feedback loop for considering the loop's stability.

impedance. The red curve of Zin shows the matching is effective until 10 MHz.

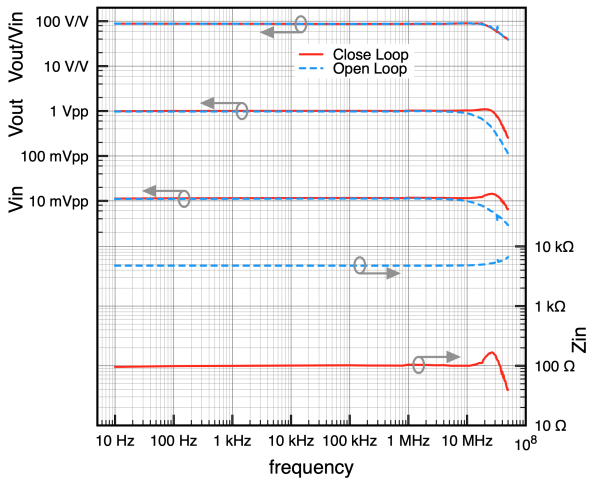

Figure 14: Measurements of LNA, from top to bottom: gain (Vout/Vin), output voltage (Vout), input voltage (Vin) and input impedance (Zin) with (red curves) and without (blue dashed curves) resistive feedback for the input matching.

Stability

Time response to a large dynamic square wave ($\approx 1\ V_{pp-diff}$) at 1 MHz shows good stability (Figure 15).

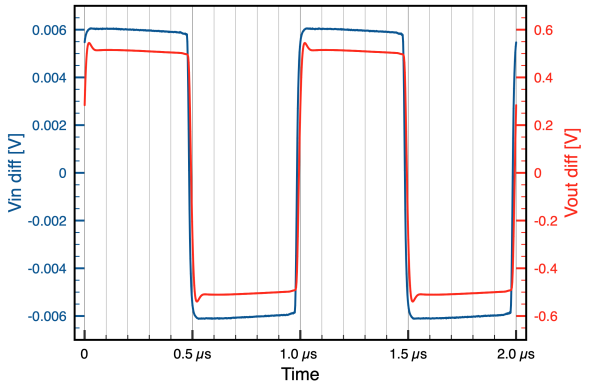

Figure 15: Measured LNA output response (red curve) to 12 mVpp 1 MHz square signal at the input (blue curve).

Linearity

Quasi-static response show non-linearity lower than 1% up to 20 mVpp input signal (Figure 16).

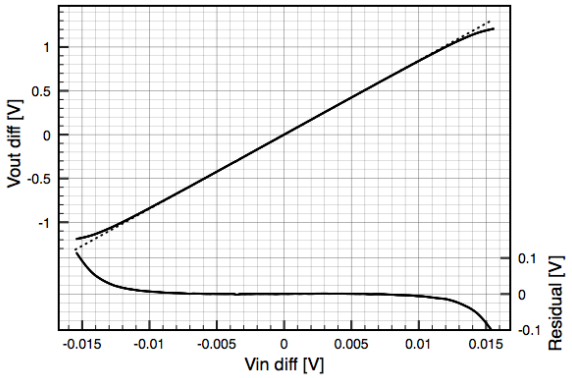

Figure 16: (top) Quasi-DC (measured at 10 kHz) Vout as function of Vin amplitude; (bottom) Residual corresponds to the ideal gain. Saturation is clearly visible at Vin > 20 mVpp and Vout > 2 Vpp. Doted-line is the ideal linear gain 84.6 V/V.

Gain drift

The LNA of "AwaXe_v3" uses a current reference PTAT for bias, namely the current is proportional to temperature. It allows to mitigate the variation of transconductance g_m, then produces a more stable gain. The Figure 17 illustrates the gain drift of the LNA between -25 °C and 75 °C. The top curves are the measured and simulated gain and the bottom ones are the gain drift. The LNA is capable of keeping gain drift smaller than 200 ppm/K from 24 °C to 64 °C, and smaller than 350 ppm/K from about 11 °C up to over 75 °C.

Current source/DAC

This section for now uses simulations to illustrate the performance of DAC and current sources. Nevertheless, the simulation

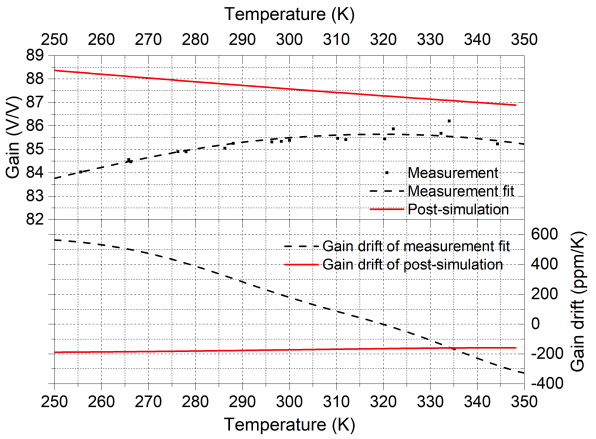

Figure 17: Gain drift versus temperature variation: (top) Gain; (bottom) Derivative of the gain, that is the gain drift with unity ppm/K or ppm/$^{\circ}C$.

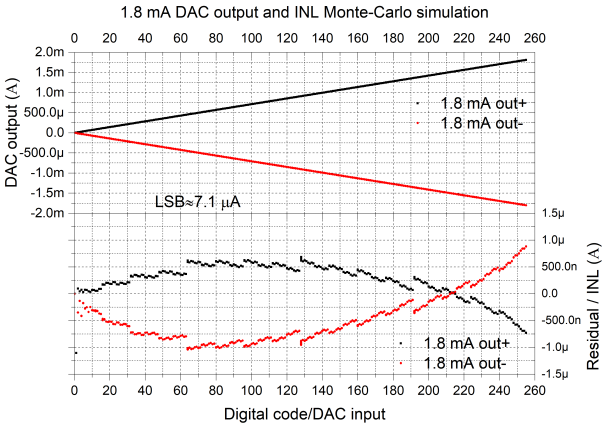

Figure 18: (Top) Monte-Carlo simulation of 1.8 mA DAC showing the positive and negative output of 256 levels; (Bottom) Residuals are all significantly smaller than the LSB 7.1 μA.

results are generally very coherent with measurement according to the characterisation of the last versions ASICs.

Output & INL (Integral Non-Linearity)

Figure 18 is the simulation of 1.8 mA DAC with all 256 levels ([0, 1.8 mA]) positive and negative output on the top and corresponding INL(residual) on the bottom. For an LSB about 7.1 μA, the maximum residual is smaller than 1 μA, namely about 0.14 LSB.

Output current noise

Figure 19 shows the simulated output current noise of 1.8 mA and 300 μA DACs, both with 3 levels of output: LSB, MSB and maximum current. A capacitor of 100 μF along with a 100 Ω resistor is connected at the output of the current reference (as illustrated in Figure 1, between I_{out} of the reference and I_{in} of an NMOS fanout current mirror) for the simulation to filter the reference output noise down to 100 Hz.

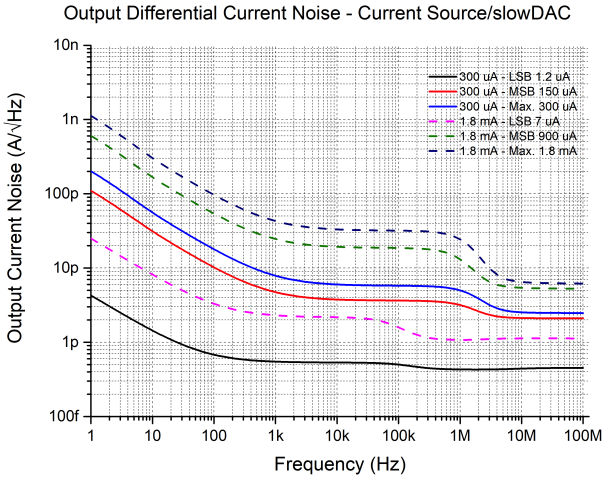

Figure 19: Output current noise of 1.8 mA and 300 μA DACs, both with 3 levels of output: LSB 1.2 μA, MSB 150 μA and maximum current 300 μA for 300 μA DAC and LSB≈7 μA, MSB 900 μA and maximum current 1.8 μA for 1.8 μA DAC.

AC Output impedance

Figure 20 illustrates the simulations of AC output impedance of both 1.8 mA and 300 μA DACs with MSB. An offset of the common mode voltage at the output is also considered, with 5 levels simulated: 1 V, 1.25 V, 1.5 V, 1.75 V and

2 V, where 1.5 V is the nominal value without any offset. Moreover, differential output impedance and single-ended output impedance (positive and negative) are all simulated.

The output impedance is provided by MOSFET, which is inversely proportional to the output current. So indeed, the output impedance will vary along with the change of binary configuration bits. The differential impedance approximately equals the sum of the two single-ended impedance. The impedance has also a dependence of the common mode voltage V_{cm} at the output, especially when V_{cm} is too low, the degradation of output impedance becomes evident.

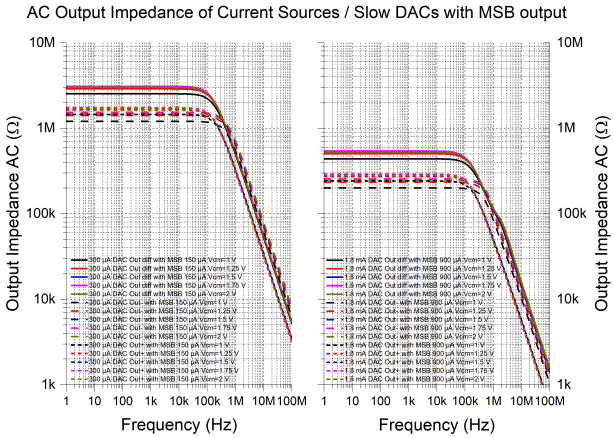

Figure 20: AC output impedance (Left) 300 μA DACs with MSB; (Right) 1.8 mA DACs with MSB. 5 levels of common mode voltage at output were simulated: 1 V, 1.25 V, 1.5 V, 1.75 V and 2 V. Solid lines: differential output impedance; long dashed lines: impedance of the negative output; short dashed lines: impedance of the positive output.

DAC with fixed current source

Output & INL

The fixed current sources integrated in "AwaXe_v3" provide a second possible output range, which is demonstrated in Figure 21 using Monte-Carlo simulation. The two outputs of a 1.8 mA DAC combining with an opposite fixed current source of 1.8 mA can vary the output current between -1.8 mA and 1.8 mA. Comparing to the simulations in Figure 18, the LSB is doubled as well as the absolute residuals since two outputs of DAC are connected together. However, the maximum relative residual stays in a similar level of about 0.18 LSB (2.5 μA/14.2 μA).

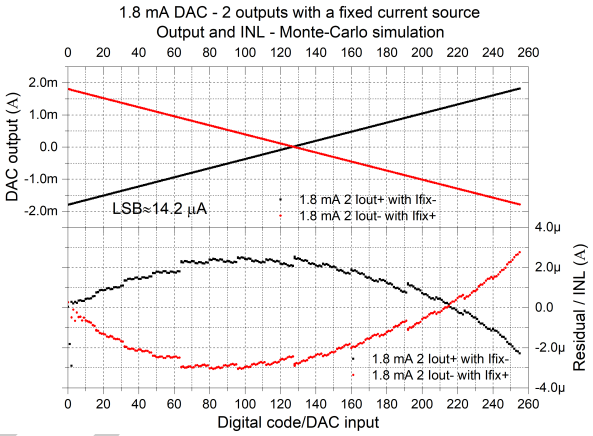

Figure 21: Monte-Carlo simulation of 1.8 mA DAC combining two outputs with an opposite fixed current source (black: 2 I_{out+} with I_{fix-} and red: 2 I_{out-} with I_{fix+}). (Top) Output of 256 levels; (Bottom) Residuals.

Output current noise

Figure 22 shows the output current noise simulation for the sources of 1.8 mA and 300 μA. The output current sums two outputs and an opposite fixed current. three levels of DAC: LSB, MSB and maximum current were simulated. For two positive outputs plus a negative fixed source:

- 2 LSB + I_{fix}: $I_{out} \approx$ -1.8 mA;
- 2 MSB + I_{fix}: I_{out} is close to 0;
- 2 Max. + I_{fix}: $I_{out} \approx$ 1.8 mA.

For two negative outputs plus a positive fixed source, the output is thus the opposite.

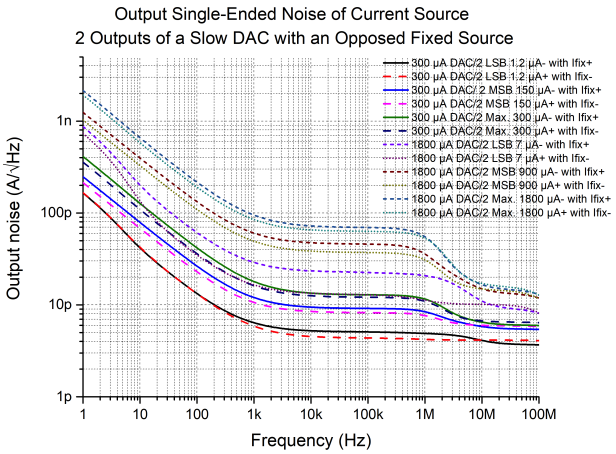

Figure 22: Output current noise of 1.8 mA and 300 μA DACs with a fixed current source, both with three levels of DAC's output: LSB, MSB and maximum current.

RS485/I^{2}C bus

The verification of the series bus RS485/I^{2}C used an 8-bit micro-controller from Microchip: "PIC18F46J50" together with "MAX13432" RS485 drivers. The device is powered and controlled via an USB 2.0 interface. The ASIC must be powered separately and before plugging the USB device. The real-time firmware running on the "PIC18F46J50" can send a Read or a Write frame to any I^{2}C device address at 400 kHz. It has been developed as bare-metal programming. The firmware can be reprogrammed into the "PIC18F46J50" via a "PICKIT3" or via the USB (using HIDbootloader). When the test device is powered-on with its push-button pressed, it enters the USB-reprogrammable mode. Otherwise it stays in normal operation mode. Any Computer can send orders to the device as a USB bulk frame, using for example libusb.

Figures 23 and 24 show respectively the measurements of "read" and "write" function of the series bus integrated into the ASIC "AwaXe_v2.5". The decoders in "AwaXe_v3" are exactly the same as in "AwaXe_v2.5" except the addresses, so their behaviours should stay the same. The RS485/I^{2}C interface of the ASIC has a differential voltage lower than the testing kit. It can be clearly seen in Figure 23: The data is written on the bus by an I^{2}C decoder in the ASIC, with a lower amplitude than the address written by the master. In Figure 24, both address and data are written by the master, so they have the same amplitude.

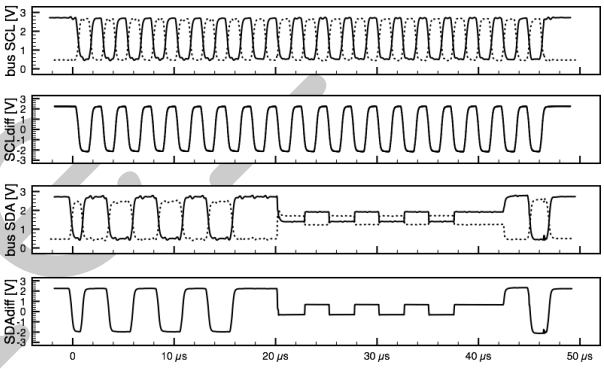

Figure 23: I^{2}C read measurement

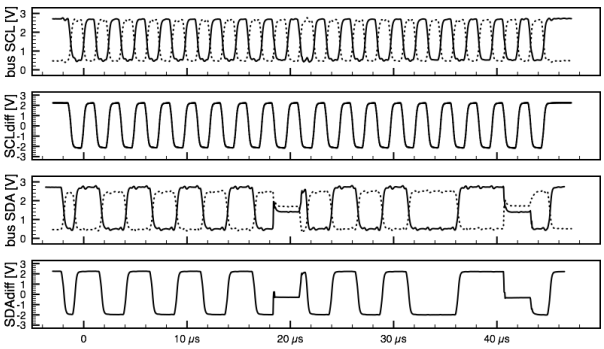

Figure 24: I^{2}C write measurement

Thermometer

Measured differential voltage of the on-chip thermometer as function of the chip temperature is shown in Figure 25.

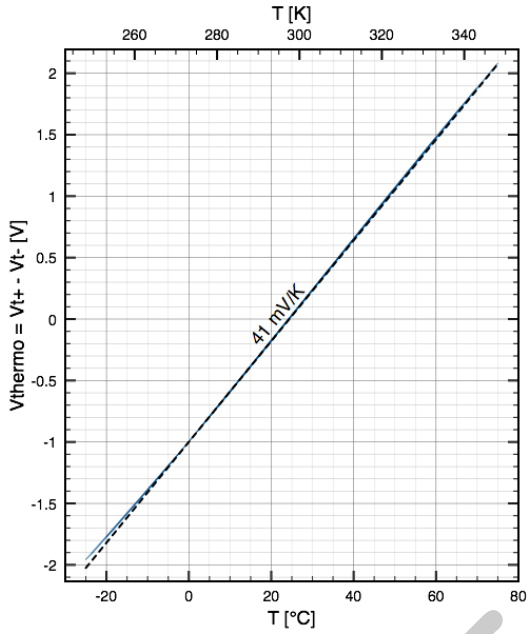

Figure 25: Differential voltage Vt+-Vt- of the thermometer loaded by two 3.3 kΩ resistors connected to Vcm. Dashed line: Measured with Rptat = 300 Ω and Rctat = 6810 Ω. Solid line: model Vt+-Vt- = 57 mV/°C ×(T-22 °C)

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VERSION

- Version 1.0, 07/10/2020