APC, AstroParticule et Cosmologie, Université Paris Diderot, CNRS/IN2P3, CEA/Irfu, Observatoire de Paris, Sorbonne Paris Cité, 10, rue Alice Domon et Léonie Duquet, 75205 Paris Cedex 13, France

WFEE Power budgets update (including buffers)

	Name & Society	Date	Signature
Prepared by	**Damien Prêle**	**22/06/2021**	
To be checked by			
Authorized by			

INDEXATION NOTE

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AUTHORS: **D. Prêle**
SUMMARY: buffers are now expected to be include in the 2 FB lines /ch and 13 row addressing lines / 1/6WFEE. More, the CV are located in the DRE, so the 30% dissipation due to the CV are mainly include to the DRE power budget. So we remove any CV dissipation from the WFEE budget in this new document. However, we add the dissipation of the linear regulators used to provides the +1.65V -1.65V to the ST ASIC from a single 5V

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Context

RHF200 buffers are now expected to be include in the

- **2 FB lines /ch -> 64 /WFEE box**

and in the

- **13 row addressing lines / 1/6WFEE**

Power

- **Consumption**

The power consumption of the WFEE is mainly driven by the active devices:

- ASICs
- Buffers
- Regulators

Dissipation in the matching resistor bridge circuit and transmitted to DRE and FPA are assumed to be less than 10% of the WFEE consumption.

In the ASIC

List of active WFEE functions and their consumption (we assumed a 5V power supply, -1.5 V +3.5 V for the DM, and a +-1.65 V for the EM).

The WFEE includes 96 channels. On ASIC includes 2 of these channels. Some functions are then common to 2 channels in one ASIC. We consider here the consumption using the AwaXe_v3 :

We considered **one channel** as:

- **1 Slow DAC TES** + I2C decoder (8 mA -> 40 mW)
- **1 LNA** + current source/bias (40 mA -> 200 mW)
- **4 Slow DAC SQUIDs** + I2C decoders (4x7 mA -> 140 mW)

+ **per ASIC**:

- **1 RS485 transceiver + 10 I2C dec.** one digital bus chip (10 mA -> 50 mW)[1]
- **1 Current reference** for all the DACs of one chip + I HK (3 mA -> 15 mW)
- **1 Thermometer for chip T HK** (5 mA -> 25 mW)

The total power consumption for 96 channels in 48 ASICs is therefore:

P_Total_ASIC = 48 x P_ASIC

= 48 x [(40mW + 200mW + 140mW) x 2 + 50 mW + 15 mW + 25 mW]

= 48 x 850 mW

~ 41 W

Integrating 20 % for margins (8.2 W):

ASIC consumption = 50 W

In the Buffer

The considered buffers are the RHF200. From the datasheet, the consumption is in between 105 mW typ. to 135 mW max. There is 2 buffers per channel in the feedback lines. So 2 x 96 buffers for all feedbacks. In addition, the row addressing function requires 13 buffers per 1/6WFEE. So, 6 x 13 buffers more. So, including 6 x 13 row@ buffers in addition to the 2 x 96 fb buffers, the total number of buffer located in the WFEE is 270.

P_Total_RHF200 = (2 x 96 + 6 x 13) x 105 mW

= 231 x 105 mW (typ … 135 mW max)

~ 29 W

Integrating 20 % for margins (6 W) and/or considering closer to the max value:

Buffers consumption = 35 W

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[1] The digital consumption evolves during communication (Slow Control). When no communications, the consumption is about 7-8 mA, during addressing fluctuations it goes up to 10 mA and a 15 mA pick is observed during the acknowledge of the I2C protocol (during few 10µs) every addressing DACs. The average consumption is thus estimated about 10 mA.

In the linear regulators in addition to the ΔV

The space qualified regulators are not been yet identify… however, we can anticipate an extra current of about 2 x 100 mA in addition to the voltage difference dissipated in the ASIC board regulators. So 12 x 2 x 100 mA in total.

P_extra_Regulator = (12 x 2 x 100 mA) x 5 V

~ 12 W

Integrating 20 % for margins (2.4 W)

Regulator extra consumption = 15 W

- **Dissipation**

The power dissipated in the WFEE box is very similar to the power consumption of the WFEE. Indeed, we can identify the power which is not dissipated directly in the WFEE corresponding to power transmitted to DRE, FPA:

- P @ LNA output (DRE) : 1 Vpp over 100 Ω -> - 10 mW max per channels
- P @ the 2 fb (DRE) : 2x 1 Vpp over 100 Ω -> + 20 mW max per channels
- P @ SlowDAC TES (FPA) : 1.8 mA over 40 Ω -> - 130 µW max per channels
- P @ SlowDAC SQUID (FPA) : 3 x 2 x 300 µA over 300Ω -> - 1 mW max per channels

- P @ RS485 (DRE) : 2 x 3.3 V over 120 Ω -> + 180 mW per 16 channels (only during DAC setting)

- P @ row@ (DRE) : 3 x 13 x 1 Vpp over 100 Ω -> + 390 mW max in total

At the end, about 2.5 W (10 mW x 96 + 6 x 180 mW + 390 mW) is assumed to be dissipated in the WFEE in addition to the WFEE comsumption.

CONCLUSION

The total main parameters budget of WFEE excluding power supply converter/CV but including Buffers and regulator:

= 50 + 35 + 15 + 1.5 ~ 100 W

- Total consumption of whole WFEE is **100 W** with 20% of margins