Warm Front End Electronic (WFEE)

Multiplexing modes and TES array workshop - 26th of September 2016, IRAP
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The WFEE in the X-IFU instrument

Warm Front End Elec.

- **SQUID bias/offset**
- **I2C serial link**
- **LNA** (1nV/√Hz, 6MHz)

Interfaces with:
FPA, DRE, ICU, PDU/RTU
Main functions

FPA/WFEE

1. TES Bias
2. SQ1 Bias
3. SQ1 Flux
4. SQ2 Out
5. Return (RTN)
6. SQ2 Flux

SRON-XIFU-SP-2016-002
WFEE architecture

3840 TES – 40 Mux
96 FDM 1MHz-6MHz

- 96 diff. channels:
  (LNA + adj. SQUID bias)

- 8 channels/ASIC
  (Application-Specific Integrated Circuit)

-> 12 ASIC

6 WFEE board with
(2 ASIC)
(in the dewar Faraday cage)
WFEE architecture

- 8 channels/ASIC (Application-Specific Integrated Circuit)

6 WFEE board with (2 ASIC)

one channel:
First ASIC: AwaXe_v1

Layout of the ASIC:

- 3 front-end LNA topologies
- + & - adj. current sources (SQUID bias)
- serial I2C protocol decoders
- + digital cells for radiation test

#2mmx2mm size
SiGe BiCMOS 0.35µm AMS via CMP
Addressed points on the WFEF

- WFEE design
- Budgets (with margins outlined and critical issues)
  - Performances
  - Mass
  - Consumption
WFEE Design

- **WFEE** mainly use the **ASIC technology** (Application Specific Integrated Circuit)
  - Optimize mass and power consumption for a given function (LNA, Current sources …)
  - Specific design reaches required performancies and put in the chip all the functions
  - layout (RadHard Design) and architecture (redundancies/voting)
  - Multiplied channels in same device, applied redundancies with no increasing of area
  - Uses a serial link to addresses many current sources on chip

- **Standard SiGe BiCMOS** technology mainly used for analog performancies
  - # 10 years perenity
  - 350 nm: not deep submicronique technology, but mainly for noise reasons, **large devices area is required**
  - “low cost” prototypique and large “know-how” on this **mature technology**

- Apart for the filtering and the supplies (3.3 V), WFEE functions are in ASICs
  - Size of the **WFEE** is mainly due to the connectors and the routing of the boards
WFEE Performances

96 Low noise amplifier:

- Gain # 100
  - *issues?
  - *depend on the linearity requirement

- Gain stability: 17 μV/V
  - *need strong optimization of the design
  - -> strong constraint on the temperature stability (ΔT < .1°)
  - *matching impedance stability, cables ??

- BW 1-6 MHz
  - *no challenge with SiGe

- < 1 nV/√Hz with a 200 Ω source resistance (SQUID array output impedance)
  - *1 nV/√Hz already reach
  - -> en goal .7 nV/Hz, in 2-3 pA/√Hz

- input dynamic range # 10 mVpp

- output # 1 Vpp

- CMRR = 60 dB

- Non-linearity: better than the SQUID stages
The mass of the WFEE is mainly driven by:
- The size of the connectors *
- The extra functions
  - supply voltage
  - filtering
  - serial link protocol converter
  - other undefined functions?

Actual size: 170 mm x 320 mm

Mass/WFEE # 3kg (# 20 kg for all channels)

Consumption/WFEE 3.3W** (# 20 W for all channels)

* increasing of the mass if strong requirement in the connectors for EMI/EMC shielding …
** increasing of the connector if extra non-integrated functions