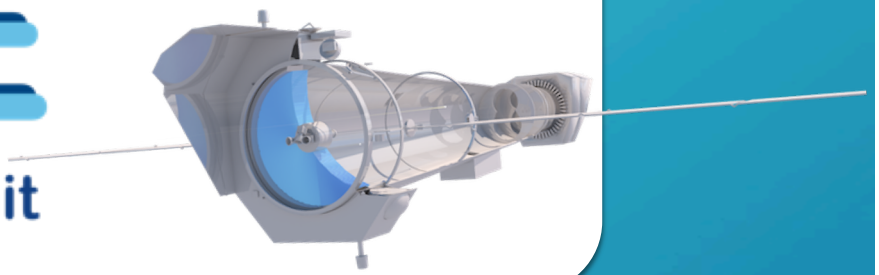
X-ray Integral Field Unit



Warm Front End Electronics

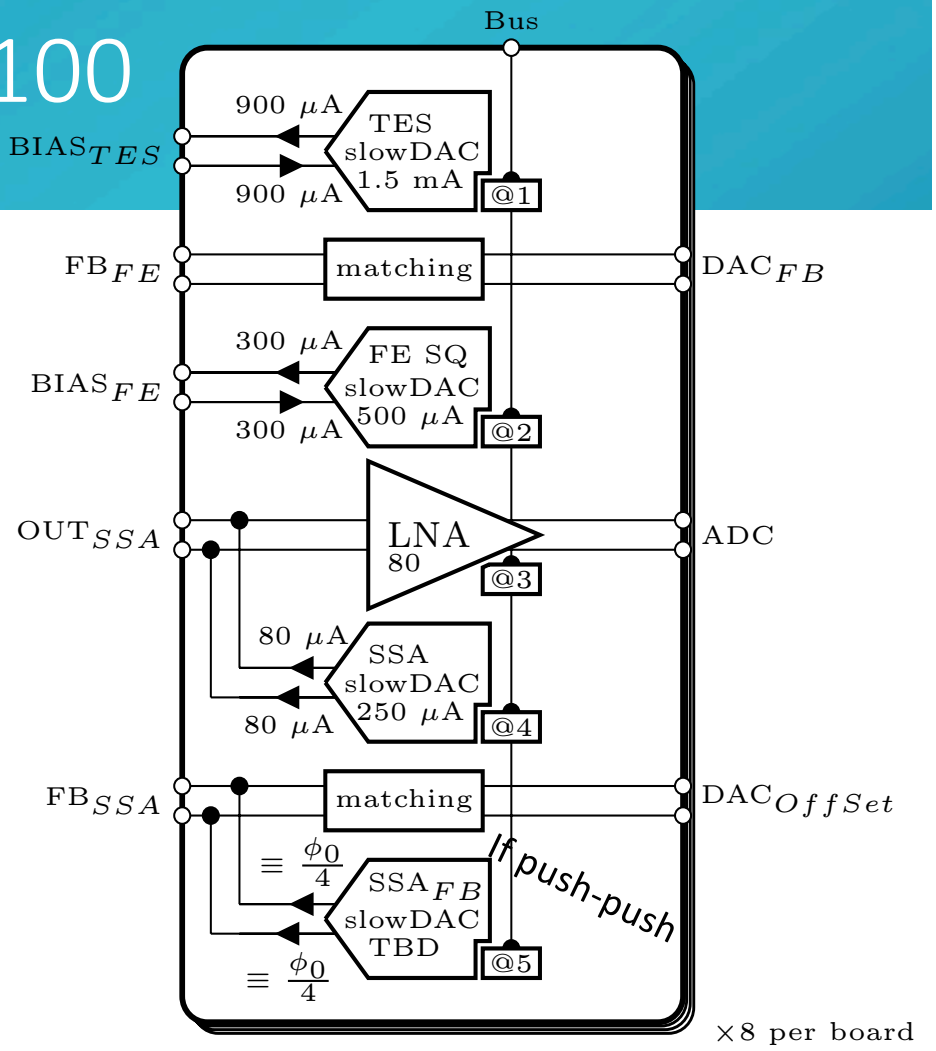
April 7, 2020 – Damien PRÊLE for the APC team

One WFEE TDM channel (main functions) x~100

1. **TES Bias** (Slow DAC Diff)
2. FE/MUX SQUID FB
3. **FE/MUX SQUID Bias** (Slow DAC Diff)
4. **LNA (Ampli)**

   Amp/SSA SQUID Bias (Slow DAC push push/pull)
5. Amp/SSA SQUID FB (Slow DAC) *Optional*

6. Current refs DAC and LNA
7. Bus I2C/RS485

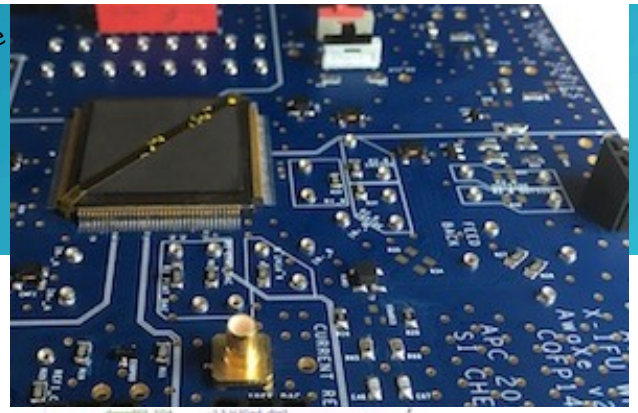


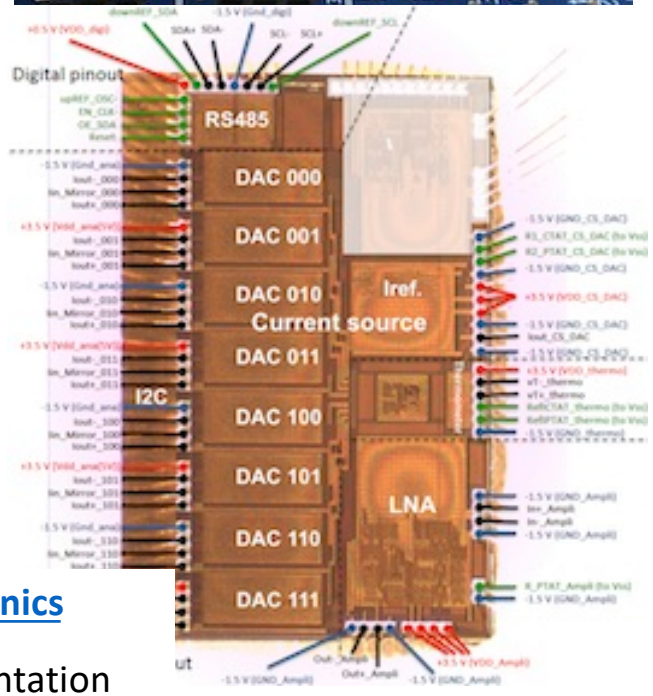
AwaXe_v2.5 FDM TDM compatible

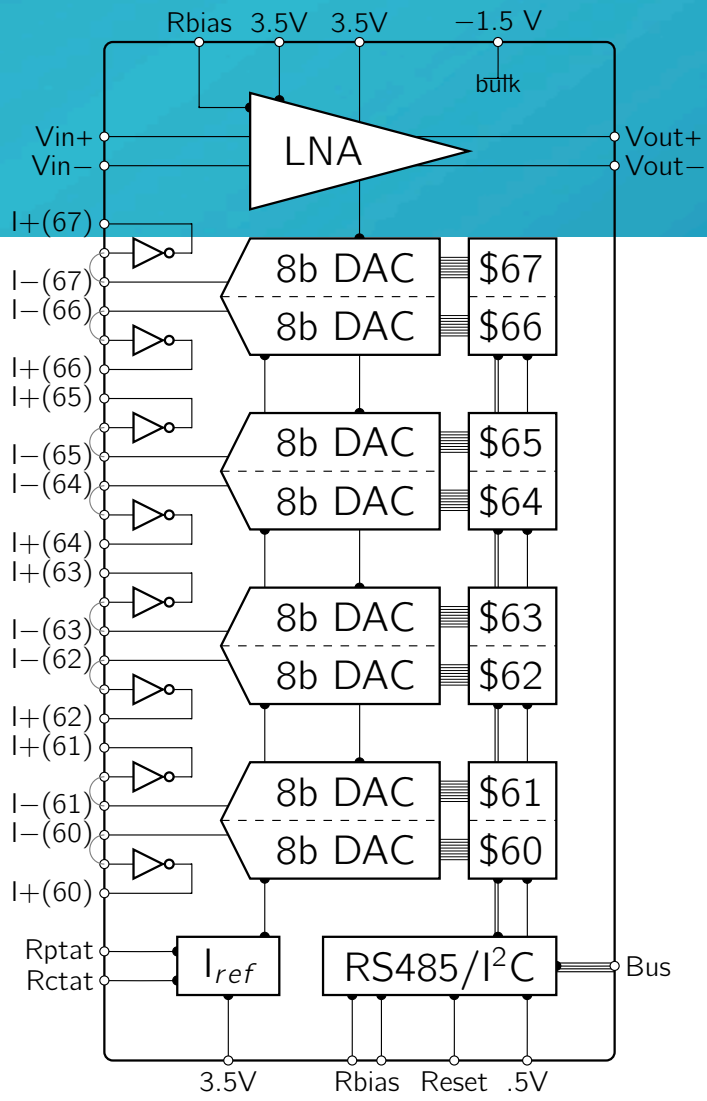
(2018-2019)

Fully operational ASIC
(based on FDM requirements)

www.apc.univ-paris7.fr/~prele/datasheet_AwaXe_v25_v20200313.pdf





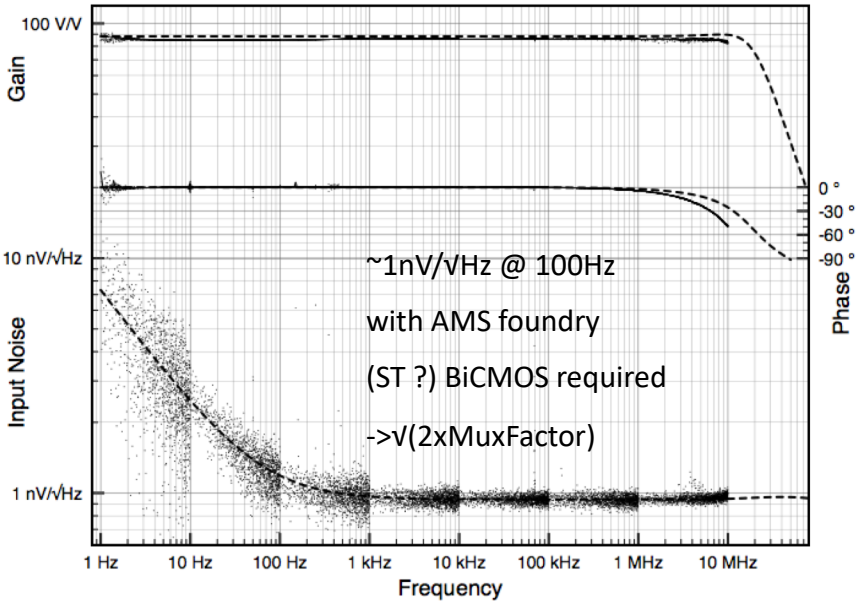


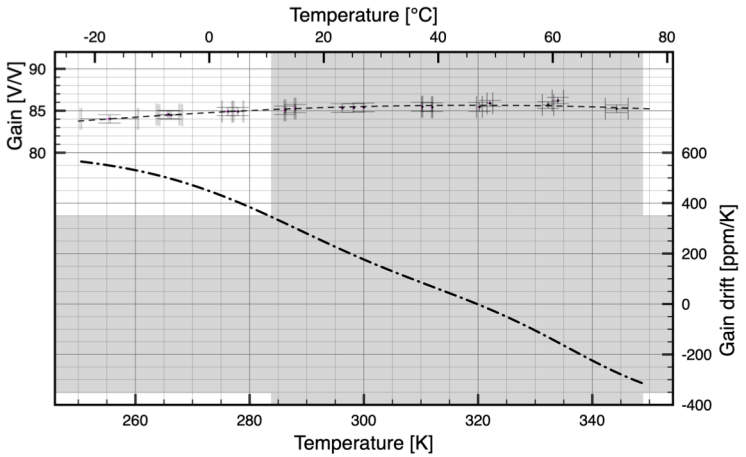
ATHENA warm ASIC for the X-IFU electronics

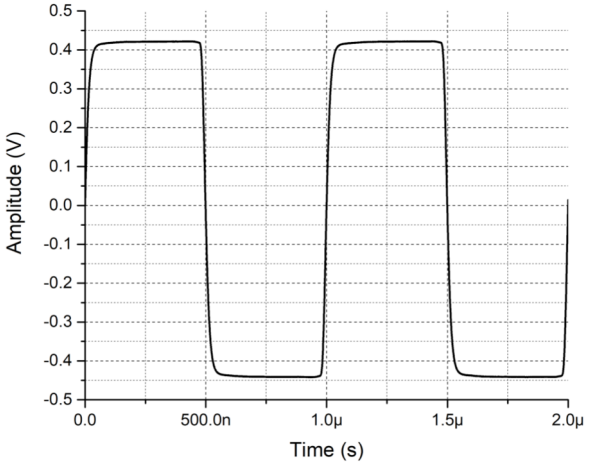
Si Chen, Damien Prêle, Bernard Courty, Fabrice Voisin, Jean Mesquida

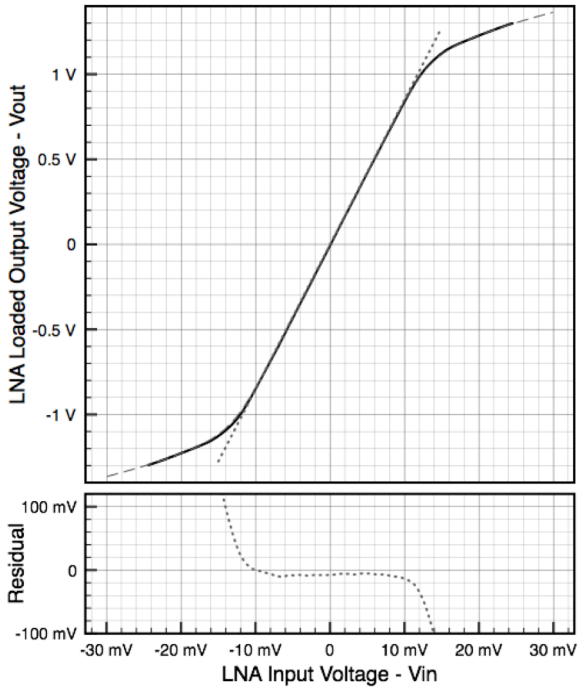
SPIE Astronomical Telescopes + Instrumentation

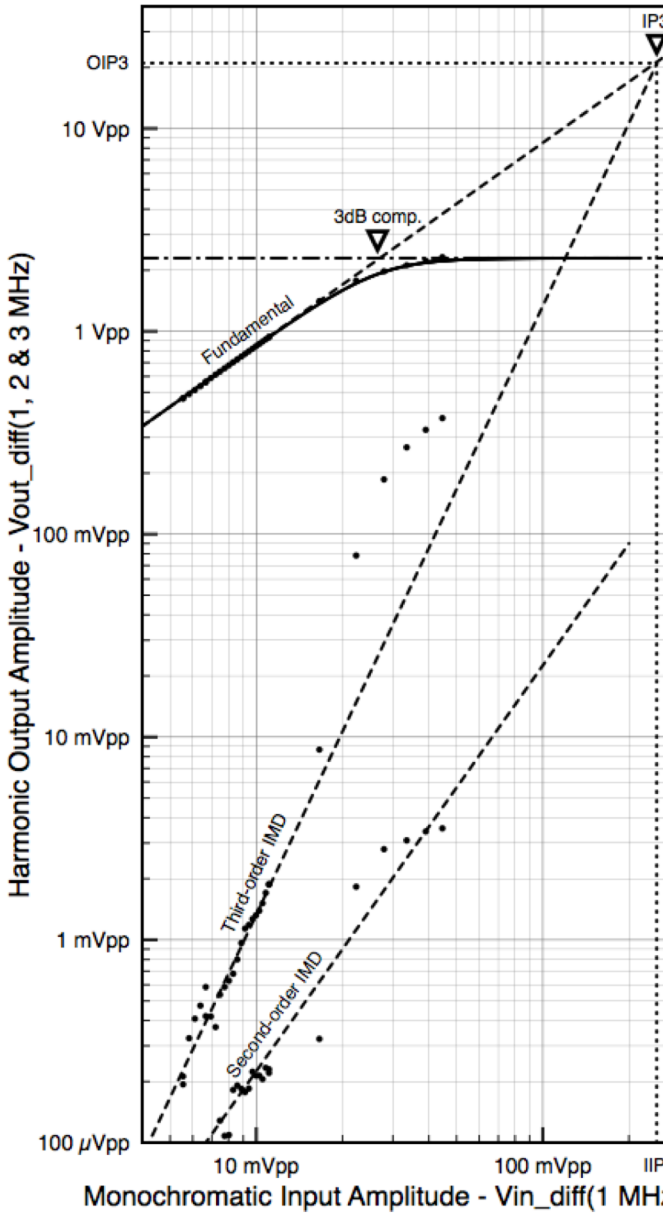
LNAv2 & 2.5 measures



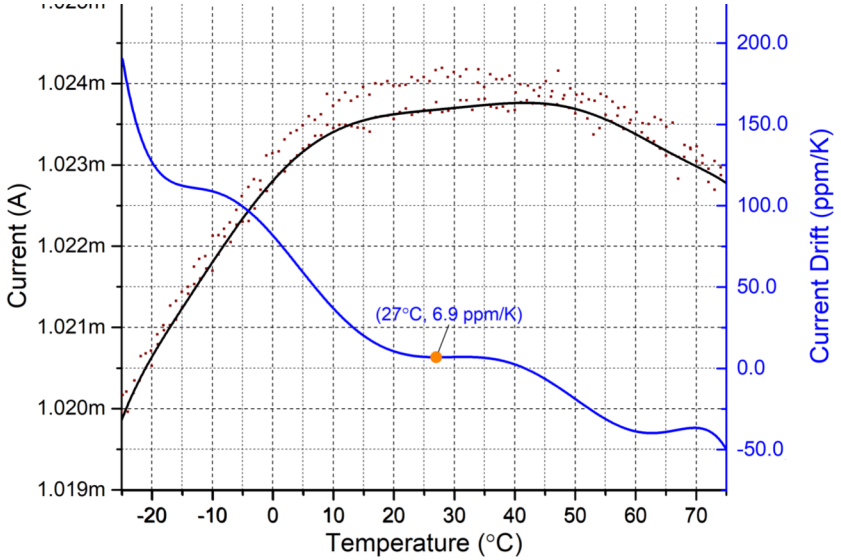


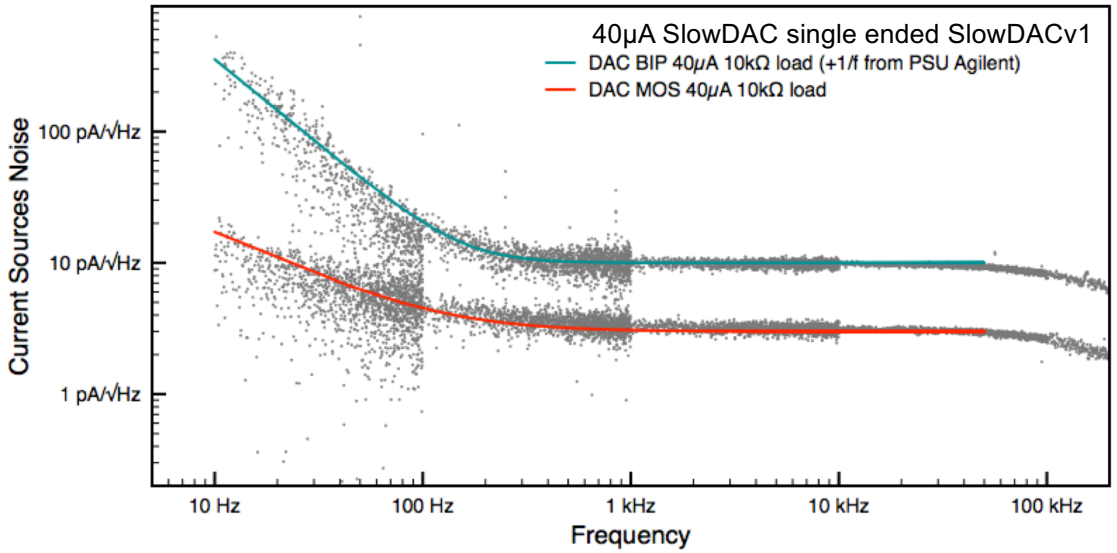


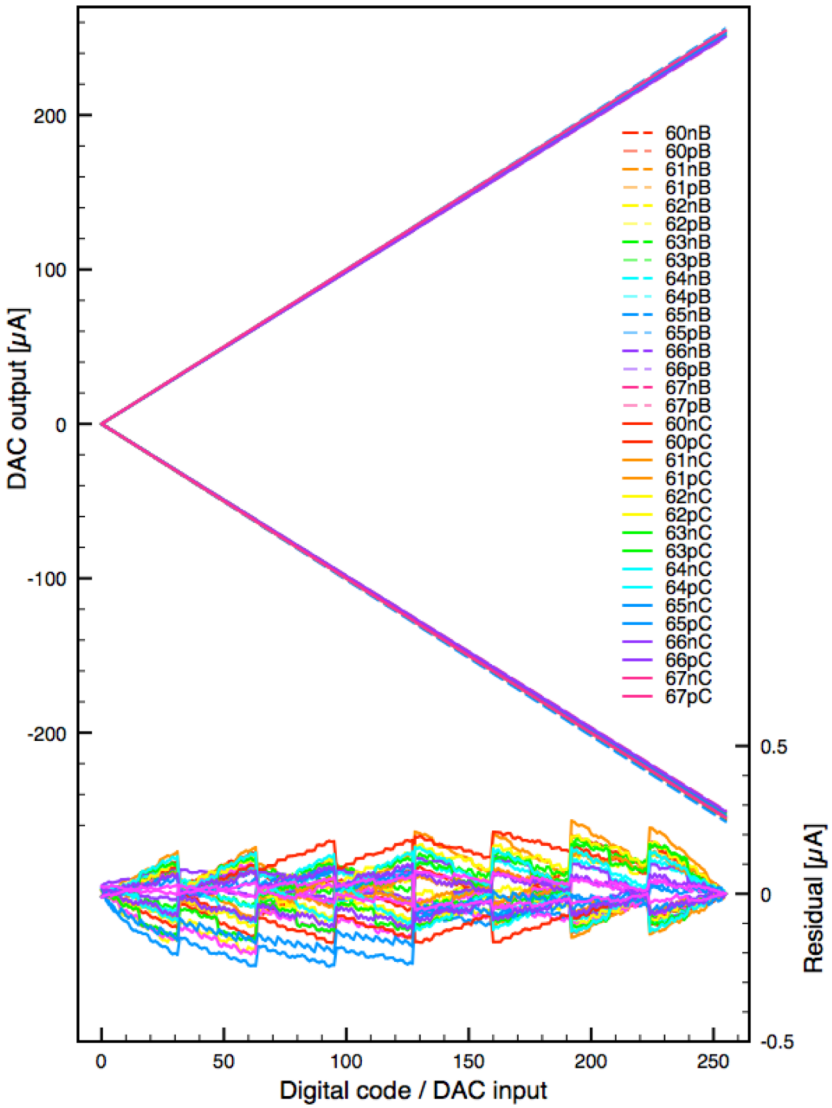




SlowDACs v2.5 measures

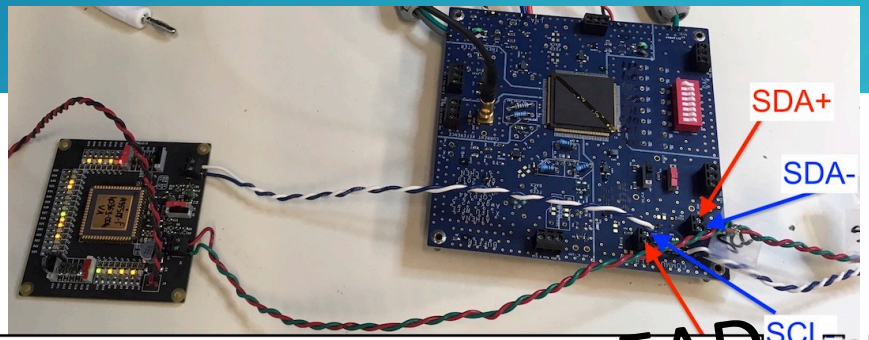




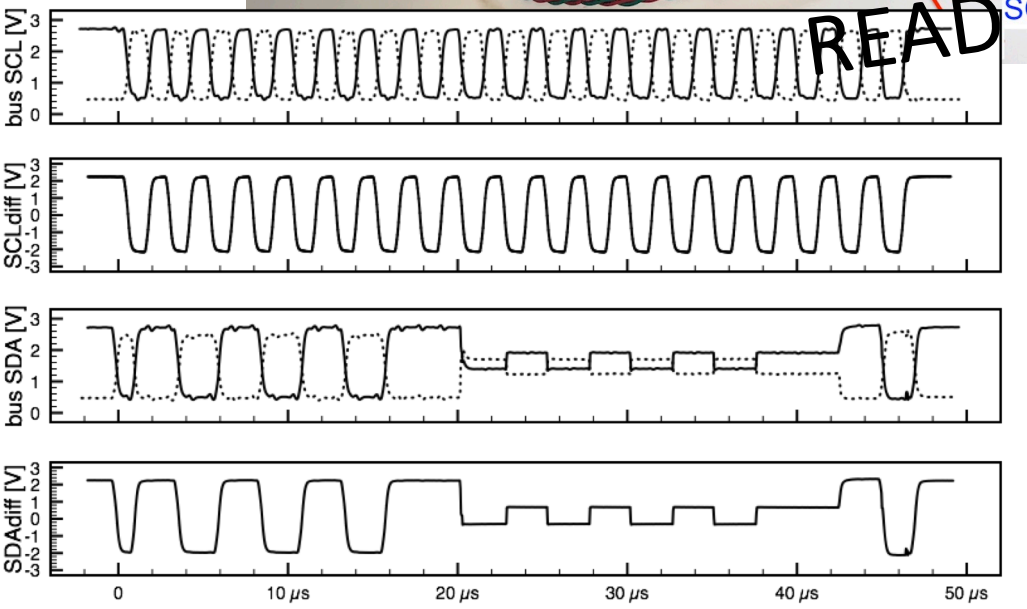


Series bus RS485/I2C

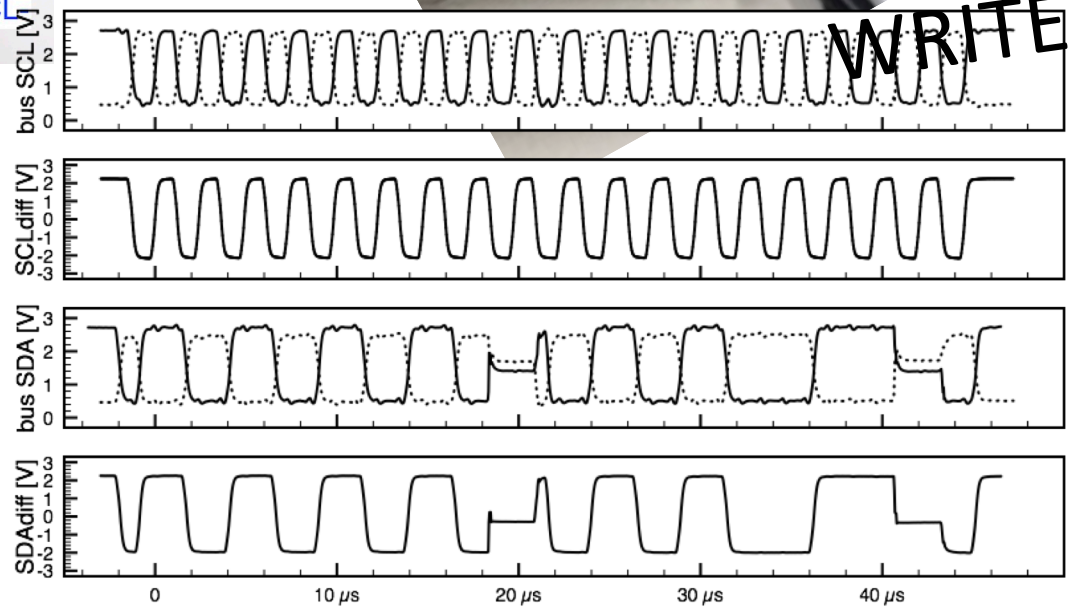
measures



READ



WRITE



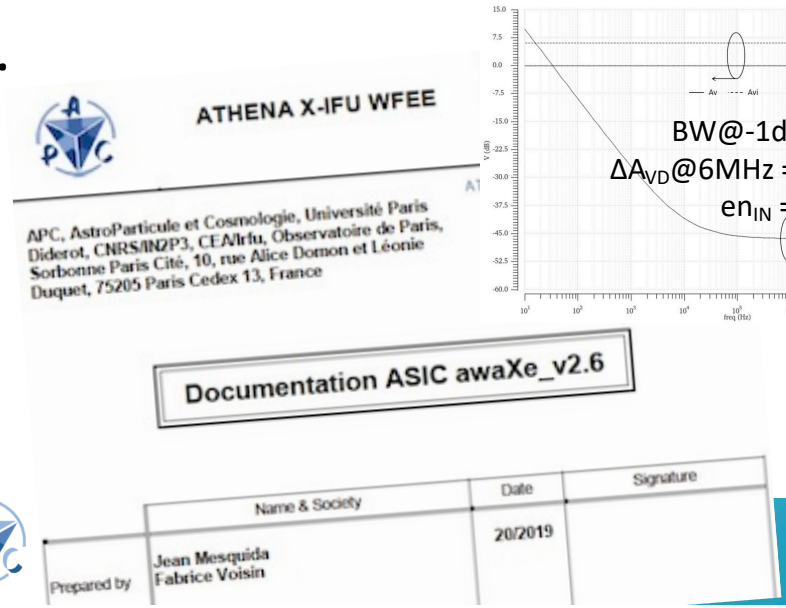
AwaXe_v2.6
(2019-2020)

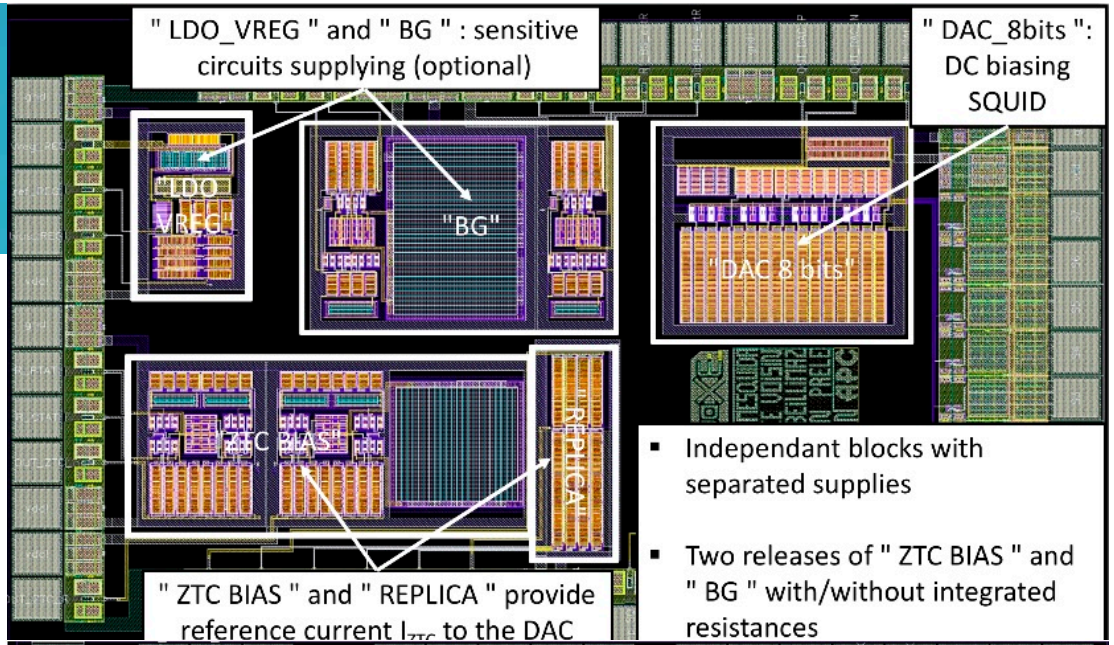
FDM
R networks
Buffer and
alternative DAC

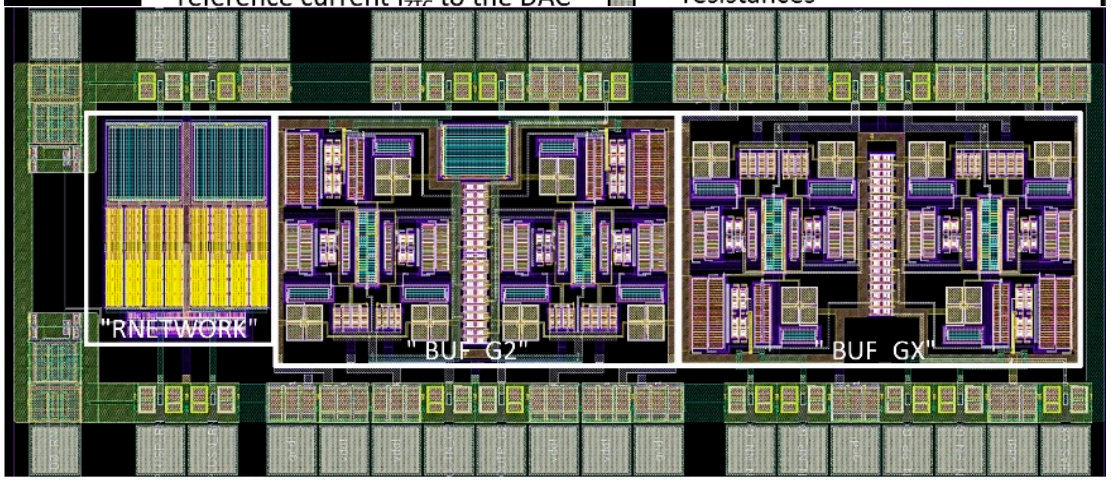
Not yet received from AMS foundry (Soon tested …)

1. **Resistor Network** for TES I(V) calibration
2. **Alternative Slow DAC** (smaller area)
3. **New Buffer topology** for bias line

…







"RNETWORK" : Network resistances diff. Adjustable voltage/current converter

"BUF_G2" : Diff. Voltage buffer with fixed gain of 2

"BUF_Gx" Diff. Voltage Buffer with no fixed gain (no internal feedback)

AwaXe_v3

(2020-2021)

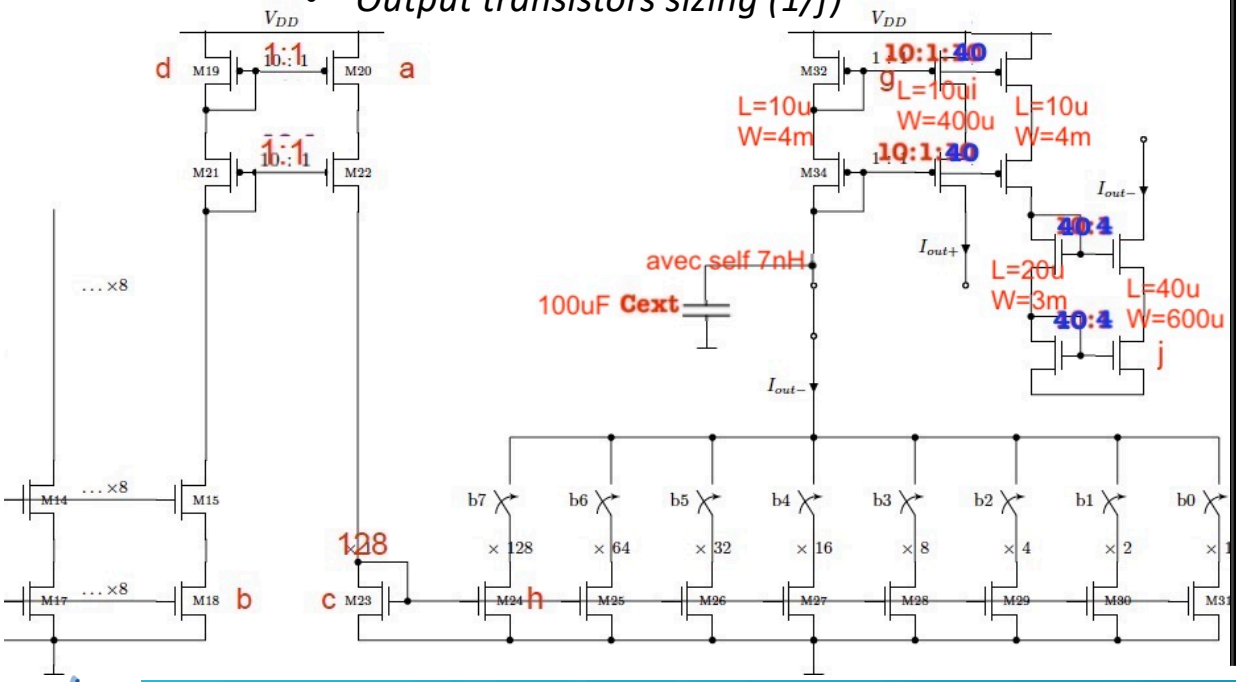
TDM

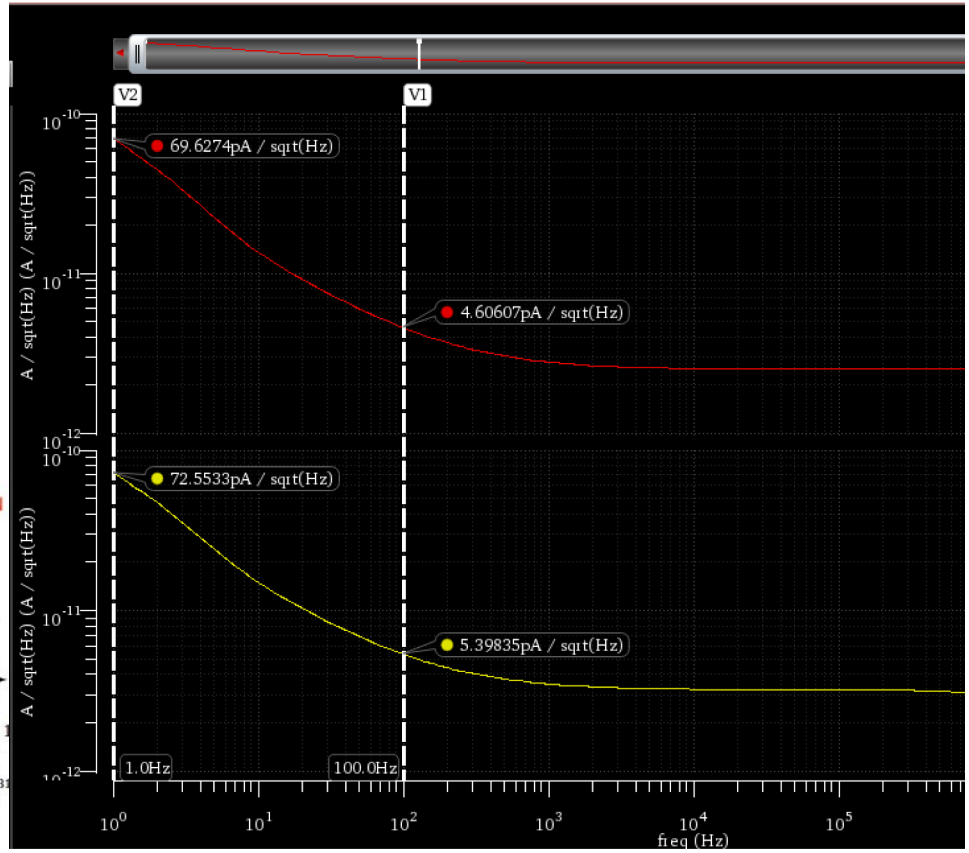
From modified v2.5 and v2.6

Reduce white AND low frequency noise

Preliminary Slow DAC modifications

- *Current mirror sizing (ref noise)*
- *External ref. filtering (ref noise)*
- *Output transistors sizing (1/f)*





New Techno ST

BiCMOS SiGe 130 nm

3 MPW runs / years
18 weeks fab.
MPW Cost 3k€/mm^2

- April 2019 :

Starting of the access request

- December 2019 :

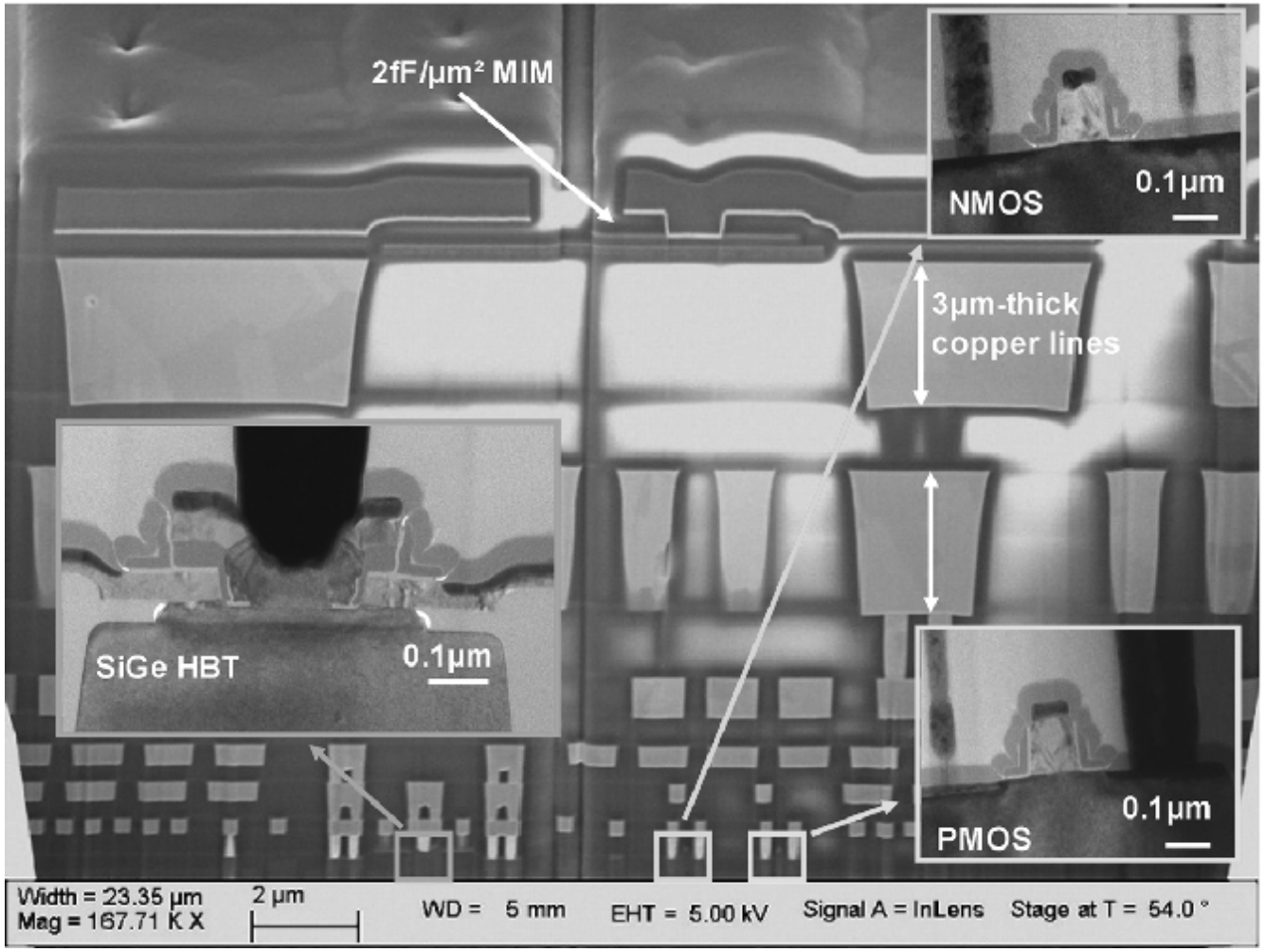
Signature of the NDA

- February 2020 :

VLAN security compliance verification

- **April 2020 :**

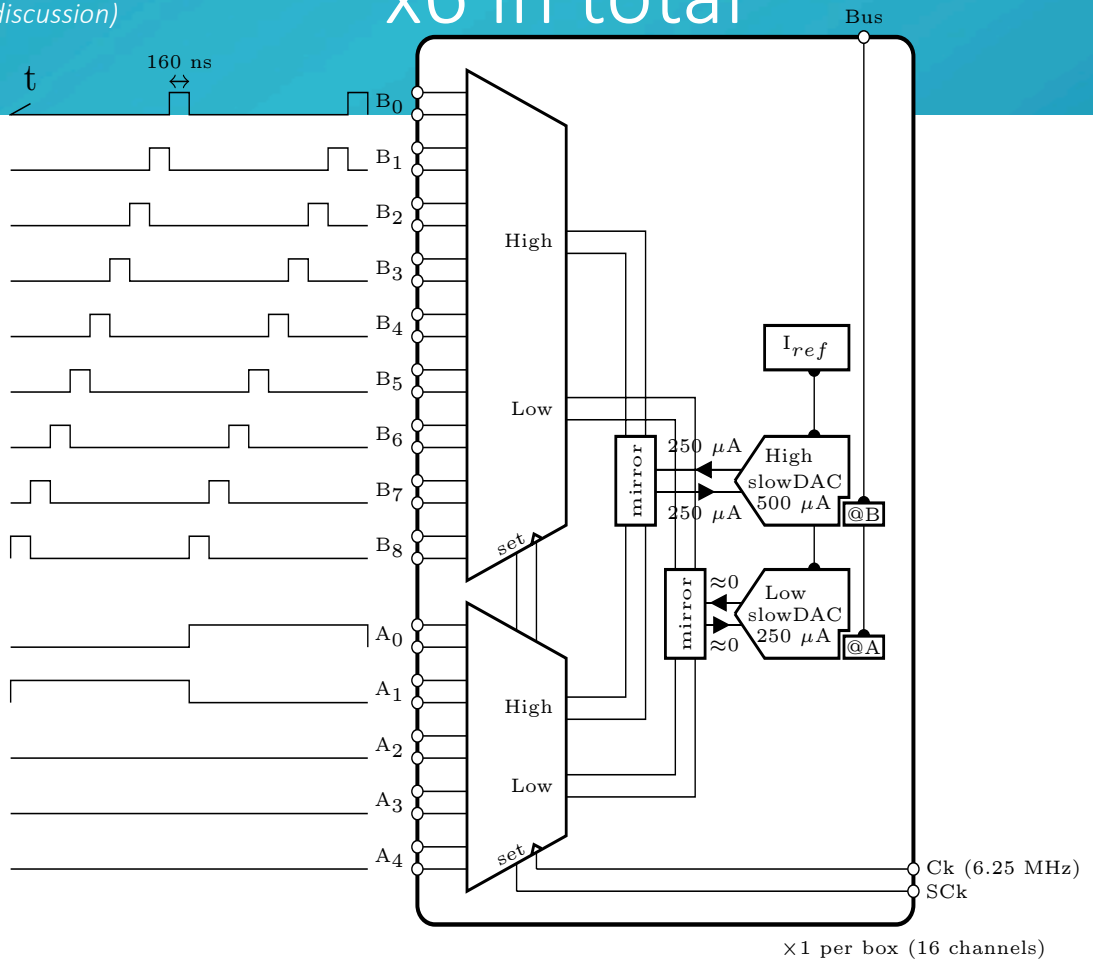
Waiting for ST approval (QUID of covid19?)



Row @ / 16 channels *(optional – under discussion)*

x6 in total

1. Demux 1/8 diff + high/Low
2. Demux 1/5 diff + high/Low
3. Slow DACs high and Low + current mirrors
4. Current refs and DACs
5. Bus I2C/RS485 (~100kHz)



Possible implementation of chapping and overlapping (fixed timing) in ASIC (?)

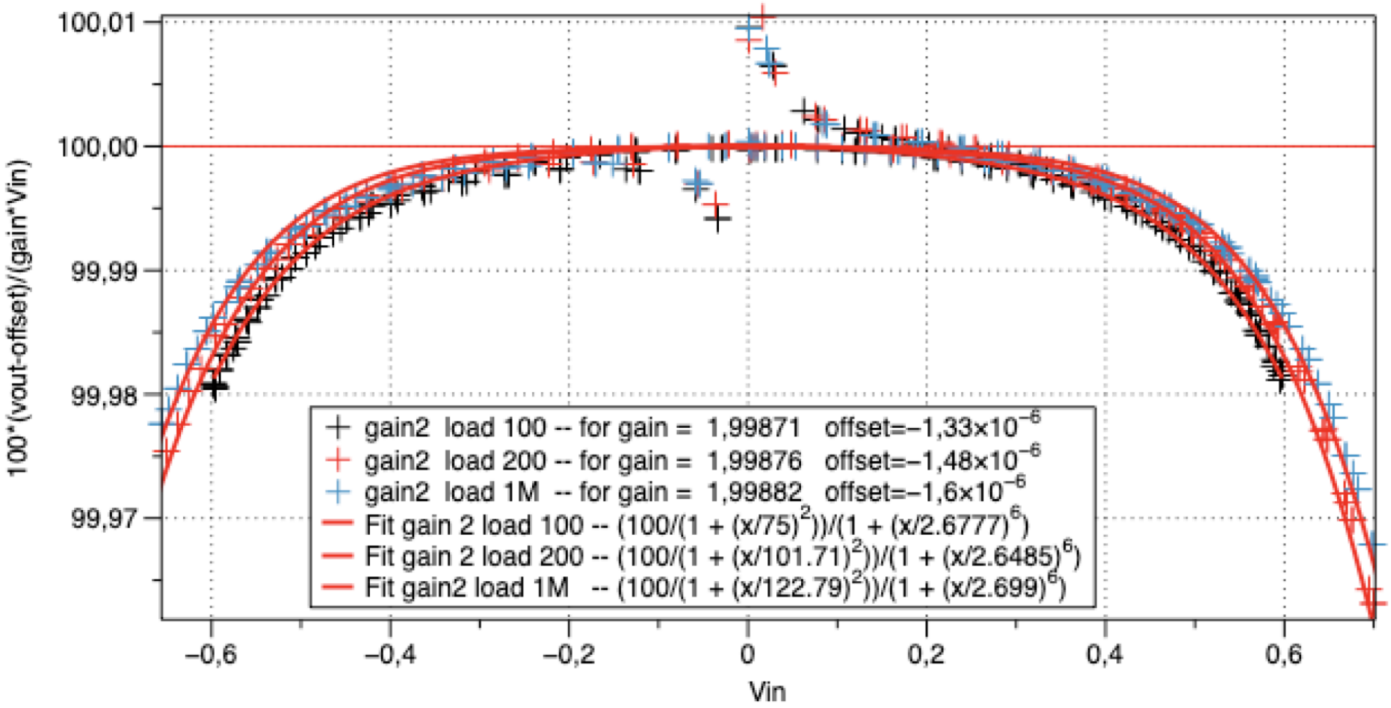
WFEE Modelization

Anticipating WFEE performances effect in the X-IFU readout chain

- Buffer/LNA Non-linearity
  -> spurious in **FDM**
- Frequency response

In **TDM**

- **LNA low frequency noise** modelization
- **SlowDAC noise** modelization
- **Bandwidth limitations** and chapping
- Impedance matching …



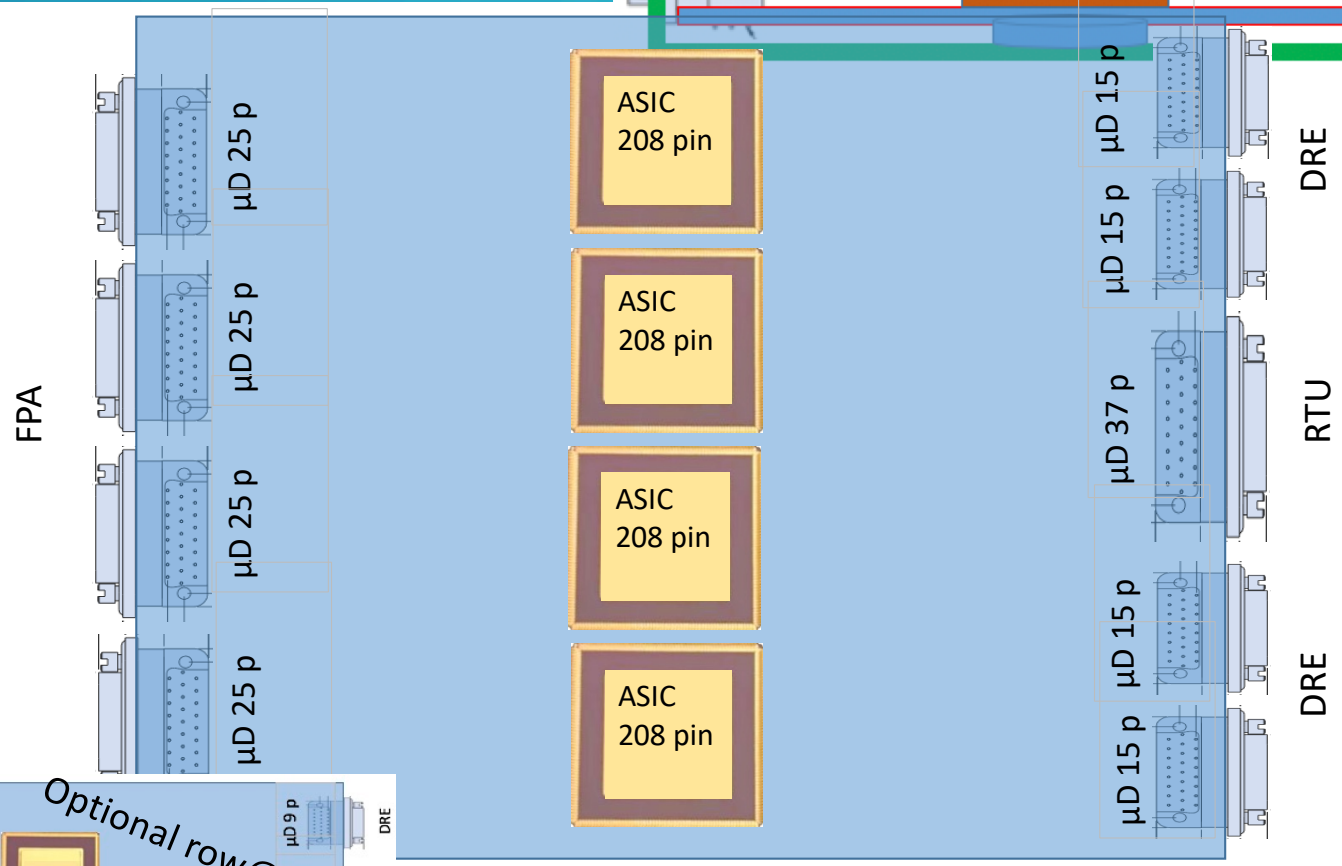
Warm front end electronic modelization for the X-IFU ATHENA readout chain simulation

Damien Prêle, Alexis Coleiro, Peggy Varniere, Si Chen, Philippe Peille, Christian Kirsch, Laurent Ravera

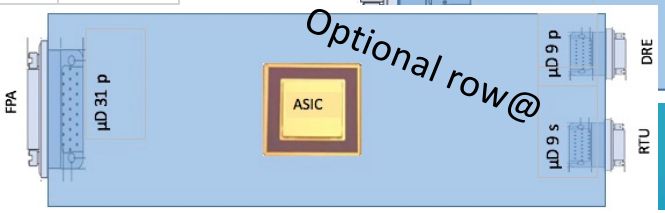
SPIE Astronomical Telescopes + Instrumentation

PCB Board design

FPA	µD 25 p
13	RTN
25	FB FE +
12	FB FE -
24	FBSSA +
11	FBSSA -
23	Bias TES +
10	Bias TES -
22	Bias FE +
9	Bias FE -
21	OUT SSA +
8	OUT SSA -
20	RTN
7	RTN
19	RTN
6	OUT SSA -
18	OUT SSA +
5	Bias FE -
17	Bias FE +
4	Bias TES -
16	Bias TES +
3	FBSSA -
15	FBSSA +
2	FB FE -
14	FB FE +
1	RTN



DRE	µD 15 p
1	RTN
9	DAC FB +
2	DAC FB-
10	DACoffset +
3	DACoffset-
11	ADC+
4	ADC-
12	RTN
5	ADC-
13	ADC+
6	DACoffset-
14	DACoffset +
7	DAC FB-
15	DAC FB +
8	RTN



	RTU
1	**mGnd**
20	**mGnd**
2	V+ (ship1)
21	V-(ship1)
3	I+ (ship1)
22	I- (ship1)
4	T+(ship1)
23	T-(ship1)
5	**mGnd**
24	V+ (ship2)
6	V-(ship2)
25	I+ (ship2)
7	I- (ship2)
26	T+(ship2)
8	T-(ship2)
27	**mGnd**
10	V+ (ship3)
28	V-(ship3)
11	I+ (ship3)
29	I- (ship3)
12	T+(ship3)
30	T-(ship3)
13	**mGnd**
31	V+ (ship4)
14	V-(ship4)
32	I+ (ship4)
15	I- (ship4)
33	T+(ship4)
16	T-(ship4)
34	**mGnd**
17	SCL+
35	SCL-
18	SDA+
36	SDA-
19	**mGnd**
37	RTN

Thermal Dissipation

Warm Front End Electronic (WFEE X-IFU ATHENA) thermo-mechanical analysis

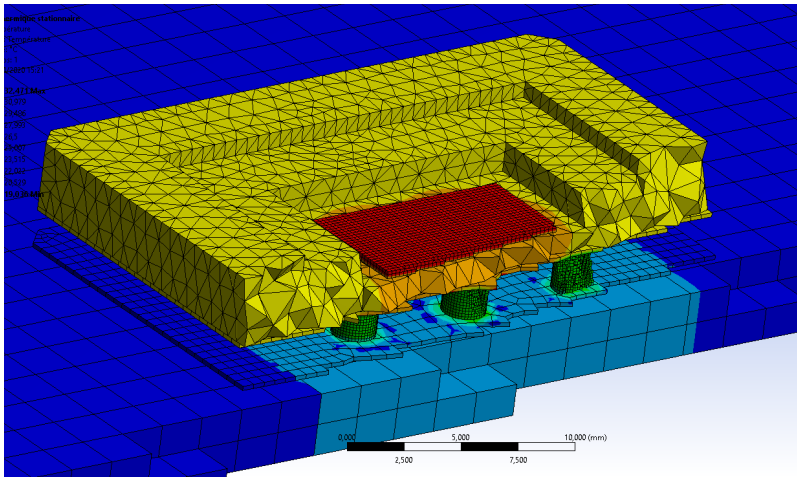
Alain Givaudan, Ardellier-Desages Florence, Prele Damien, Lesrel Jean, Oger Ronan

SPIE Astronomical Telescopes + Instrumentation

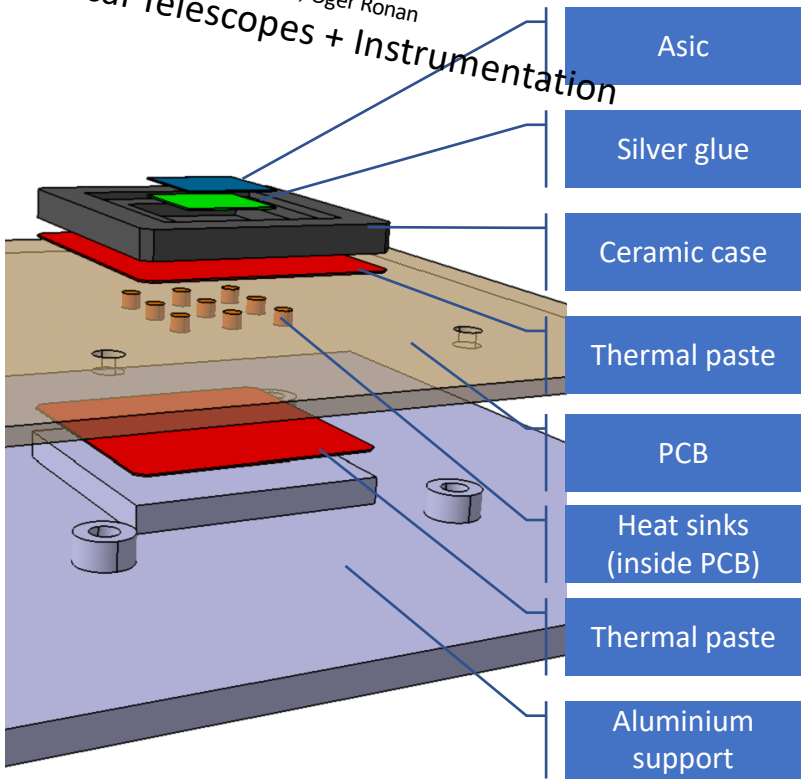
ASIC heat dissipation with heat sinks

- FEM analysis
- Thermal tests to confirmed the analysis

No radiative exchange implemented

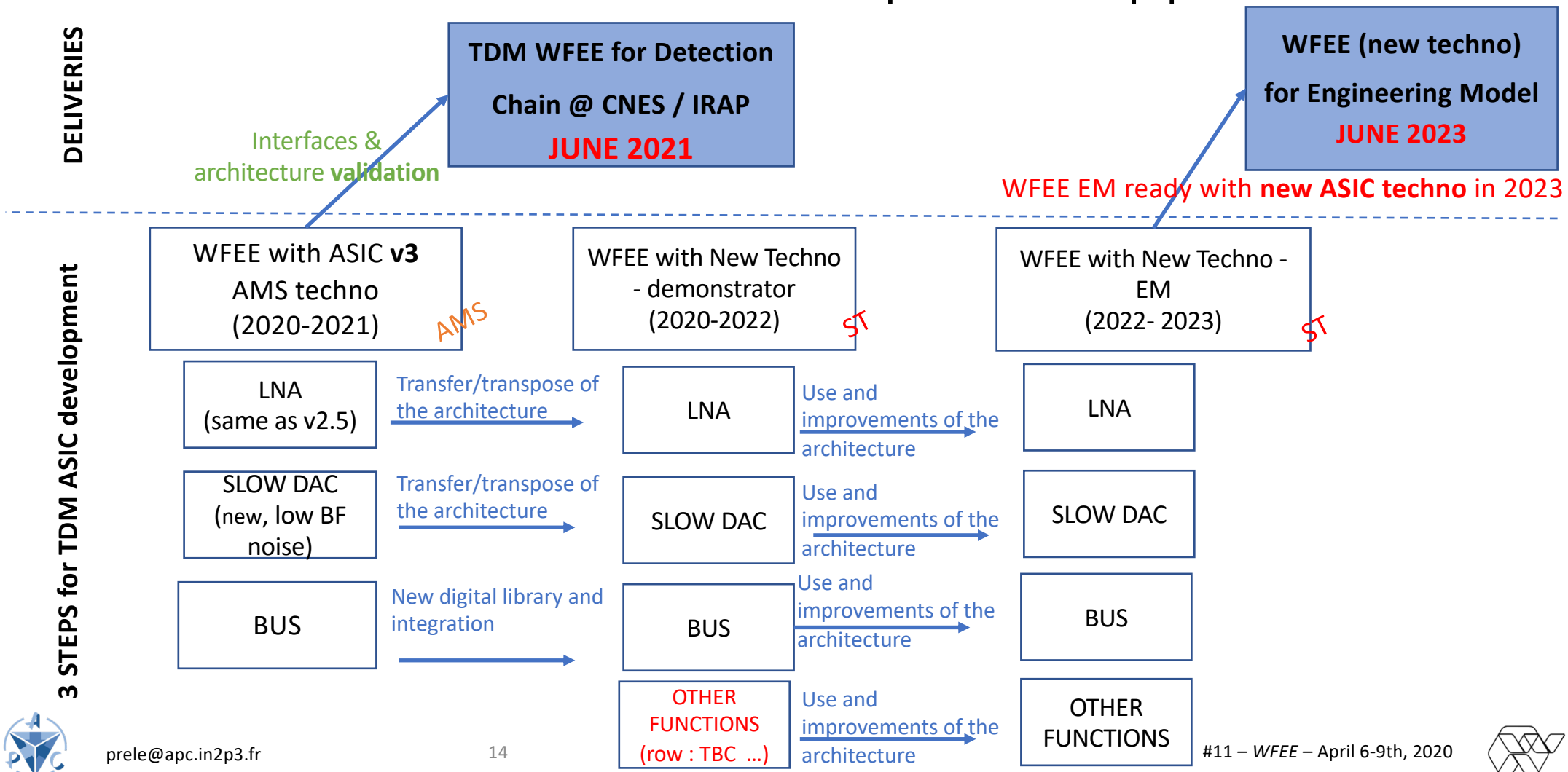


Sectional view of a thermal analysis



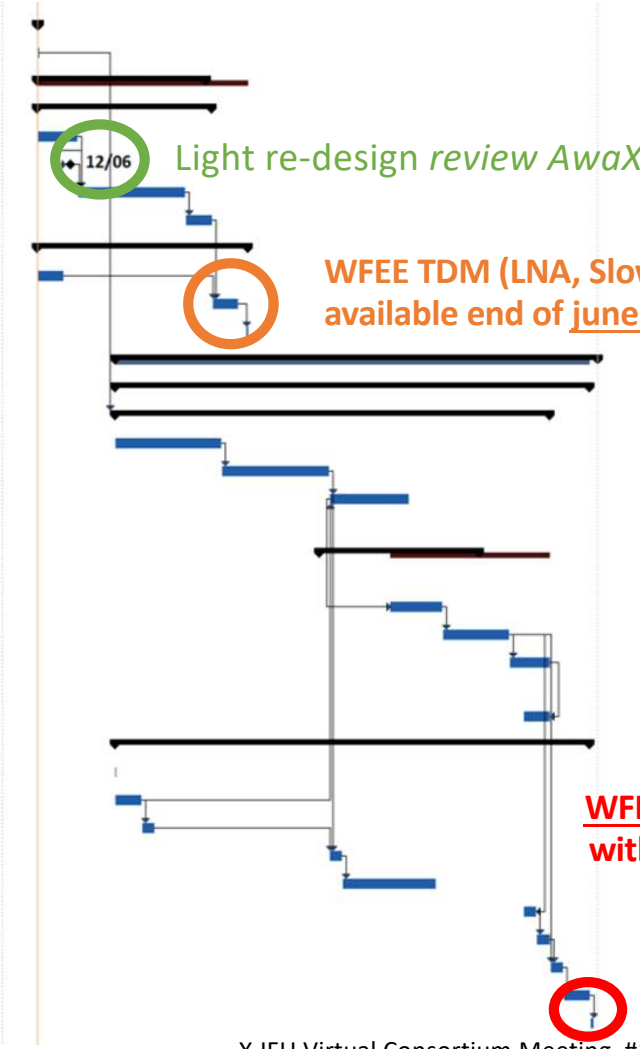
Explode CAD view of the thermal model

Main TDM WFEE ASIC development approach



TDM WFEE Time schedule for Early Demonstrator Model & EM

WFEE TDM	**2 jour:**	**Ven 03/04/20**	**Lun 06/04/20**	
Kick Off meeting	2 jour:	Ven 03/04/20	Lun 06/04/20	
Early Verification Model	**252 jo**	**Ven 03/04/20**	**Lun 22/03/21**	
ASIC v3	**261 jo**	**Ven 03/04/20**	**Ven 02/04/21**	
LNA, Slow DAC, Bus design	12 sm	Ven 03/04/20	Jeu 25/06/20	
Light Design Review	1 jour	Ven 12/06/20	Ven 12/06/20	6FD-10
ASIC AMS AwaXe v3 fundery / packaging	8 mois	Lun 29/06/20	Ven 05/02/21	6;7FD+
ASIC v3 characterisation at APC	2 mois	Lun 08/02/21	Ven 02/04/21	8
ASIC v3 PCB	**316 jo**	**Ven 03/04/20**	**Ven 18/06/21**	
design & rooting	2 mois	Ven 03/04/20	Jeu 28/05/20	
integration	2 mois	Lun 05/04/21	Ven 28/05/21	11;9
Delivery to CNES / IRAP	1 sm	Lun 14/06/21	Ven 18/06/21	12FD+2
Engineering Model	**722 jo**	**Lun 14/09/20**	**Mar 20/06/23**	
ASIC ST (new technology)	**710 jo**	**Lun 14/09/20**	**Ven 02/06/23**	
ASIC ST v1 (périmètre à définir)	**650 jo**	**Lun 14/09/20**	**Ven 10/03/23**	**3**
Design ASIC ST v1	8 mois	Lun 14/09/20	Ven 23/04/21	
ASIC ST v1 fundery & packaging	8 mois	Lun 26/04/21	Ven 03/12/21	17
ASIC ST v1 characterisation &radiation tests	120 jours	Lun 06/12/21	Ven 20/05/22	18;27
ST ASIC Design run 2 (périmètre à définir)	**240 jours**	**Lun 15/11/21**	**Ven 14/10/22**	
Design ASIC ST v2 (improvements v1)	4 mois	Lun 11/04/22	Ven 29/07/22	19DD+
ST v2 Foundry / packaging	5 mois	Lun 01/08/22	Ven 16/12/22	21
Caracterisation Measurements ST run 2	3 mois	Lun 19/12/22	Ven 10/03/23	22
Qualification Radiation ST run2	2 mois	Lun 16/01/23	Ven 10/03/23	23FF
Carte ASIC EM	**710 jo**	**Lun 14/09/20**	**Ven 02/06/23**	
ASIC ST v1 PCB	1 jour	Lun 14/09/20	Lun 14/09/20	
design & rootage_ST_v1	2 mois	Lun 14/09/20	Ven 06/11/20	
réalisation & tests_ST_v1	1 mois	Lun 09/11/20	Ven 04/12/20	27
Integration (y.c. ASIC_run1)	1 mois	Lun 06/12/21	Ven 31/12/21	28;18
caracterisation measurements_ST_v1	7 mois	Lun 03/01/22	Ven 15/07/22	29
design & rootage_ST_v2	1 mois	Lun 16/01/23	Ven 10/02/23	22FF+2
réalisation & tests_ST_v2	1 mois	Lun 13/02/23	Ven 10/03/23	31
Integration (y.c. ASIC ST_v2	4 sm	Lun 13/03/23	Ven 07/04/23	32;22
caracterisation measurements_ST_v2	2 mois	Lun 10/04/23	Ven 02/06/23	33
Delivery of WFEE Engineering Model	**1 sm**	**Lun 05/06/23**	**Ven 09/06/23**	34



Light re-design *review AwaXe_v3*: beginning June 2020

WFEE TDM (LNA, Slow DACs, Bus) with AMS techno available end of june 2021

WFEE EM (without row adressing yet included) with new techno available mid 2023

Conclusion

- Demonstrates **good performances/operations AwaXe_v2.5**
- Soon **AwaXe_v2.6 for extra functions** (R network / alter. DAC / Buffer)
- Working on **TDM shift**
- Last AMS ASIC for WFEE TDM demonstration **mid 2021 : AwaXe_v3**
- Studying the **row addressing** implementation in WFEE
- Starting the use of a **new ST BiCMOS SiGe ASIC technology** for future design