In preparation of the INFIERI First workshop:

Basic information concerning the INFIERI Workpackages (WP's)

Some reminders on INFIERI WP's
specially for PART III of the 1st workshop

These slides contain the basic information on the WP's of INFIERI project.

They are the fundamental parts of the INFIERI proposal/Annex1. These slides serve as reminder to all the INFIERI contributors and in particular for the people in charge of launching the WP's at the forthcoming INFIERI Workshop, i.e.:

- WP1: F. Palla & G. Cotter
- WP2: F. Calmon & A. Savoy-Navarro
- WP3: E. Ciaramella & N. Hessey
- WP4: Ph. Bonnot & F. Lemonnier
- WP5: R. Patti & al.
- WP6: Summary of the integration tools & test benches (all partners)
- WP7 & WP8 will be introduced as well in a separate way (see the Workshop Programme).

INFIERI Full Partnership

Partner Nb	Label	Private/ Public	Full name
1	CNRS	Public	APC: AstroParticle & Cosmology, Paris-Diderot U. INL: Institute of Nanotechnology in Lyon INSA, Ecole Centrale &ECP in Lyon.
2	FOM	Public	Nationaal Instituut voor subatomaire Fysica NIKHEF-FOM, Amsterdam
3	LIP	Public	Laboratório Instrumentação e Fisica Experimental de Partículas (LIP)
4	INFN	Public	INFN-Sezione de Pisa (S.N., U. Pisa & Siena U.)
5	UC3M	Public	U. Carlos III in Madrid (Eng. School)
6	UOXF	Public	University of Oxford
7	SSSA	Public	Scuola Superiore Sant'Anna, Pisa
8	STFC	Public	Rutherford Appleton Laboratory
9	Philips	Private	PHILIPS S.A.
10	TRT	Private	THALES Research & Technology
11	ULIV	Public	University of Liverpool

INFIERI Associated Partners

Partner Nb	Label	Private/ Public	Full name
A1	SNU	Public	Seoul National University (Prof. Soo-Bong Kim)
A2	SAMSUNG	Private	SAMSUNG SAIT, TEC & DEV Div. (InKyeong YOO, Vice-President)
A3	FNAL	Public	Fermi National Laboratory, CMS Div & LPC (Joel Butler & Ian Shipsey)
A4	PURDUE	Public	Purdue University, Physics Dept & Nanotechnology Lab. (Prof. D. Bortoletto)
A5	TEZZARON	Private	TEZZARON SemiConductor, Warrenville Ill. USA (R. Patti, President)
A6	SEDECAL	Private	Sociedad Española de Electromedicina y Calidad, Madrid (Spain) (Jose Maria Ortega)
A7	CAEN	Private	CAEN S.p.A (F. Vivaldi, Vice President)
A8	CERN	Public	European Center for Nuclear research, CH, (Sergio Bertolucci, Deputy Scientific Director)
A9	UBRIS	Public	University of Bristol (Dave Newbold)
A10	ULEIC	Public	University of Leicester (James Hinton)
A11	UvA	Public	Astronomical Institute “Anton Pannekoek” Univ. of Amsterdam (David Berge)

INFIERI Workpackages (WPs)

Work package #	WP Type	Work package title	Lead beneficiary	Start month	End month
1	RTD	Front End data processing reduction	INFN/UOXF	1	48
2	RTD	New Interconnect Technology	CNRS	1	48
3	RTD	Large flux data transmission technology	FOM/SSSA	1	48
4	RTD	Advanced Digital Processing	STFC/TRT	1	48
5	TR	Transversal Tools	ALL	1	48
6	TR	Integration studies and tests	ALL	1	48
7	TR	Training activities	ALL	1	48
8	DISS/OUT	Dissemination and Outreach	ALL	1	48
9	MGT	Consortium & Project Management	CNRS	1	48

Industrial participation to the WP's

WP No.	WP Title	Leading Industrial firms	Associated industrial firms	Expertise to be developed
1	F.E. processing and reduction	SEDECAL	CAEN	Custom digital design
2	New 3D Interconnect Packaging Tech.	TEZZARON	SAMSUNG (Collaboration. with CNRS)	vias with <50µm diameter. vias with O(1)µm diameter. & associated VDSM design
3	High rate data transmission tech.	PHILIPS	Collaboration with FOM & SSSA	New Si Photonics techno, wireless links, OWC, WDM
4	Advanced Digital data processing	TRT	SAMSUNG, CAEN, SEDECAL	Very advanced Dig. Proc. System
5	Transversal tools	IBM PHILIPS CAEN, SEDECAL	STFC (Rutherford – Appleton Lab) gives special access to EUROPRACTICE	VDSM (65nm) kits and technology access Test infrastructure
6	Integration studies & tests	CAEN PHILIPS	SAMSUNG SEDECAL	Test benches for CTA & HEP Test bench for PET
7	TRAINING	ALL industrial	ALL industrial	Specialized skills

WP1: FRONT-END DATA PROCESSING REDUCTION

presented by F. Palla &G. Cotter at INFIERI Workshop

WP1: (originality/innovative aspects)

- Introducing advanced Level-1 FEE data processing in CTA, PET or LHC instruments and thus performing in sometimes very harsh conditions from many points of view
  - ✓ an ***efficient data reduction*** and selection based on a ***real time*** understanding of the Physics or
  - ✓ the possible ***diagnoses*** the user is looking for.
- This early stage decision making implies some major technological breakthroughs in the FEE microelectronics linked to:
  - ✓ advanced PMTs or ***SiPM'***s in CTA or PET, or
  - ✓ ***advanced Si sensor technology*** at LHC.

WP2: New Interconnect Technology

presented by F. Calmon & A. Savoy-Navarro at INFIERI Workshop

WP2 purpose: to develop advanced technology in order to have the FEE or local intelligence ASIC closely embedded on the near detector element.

- This will eliminate wire or bump bonding
- improve the performance (less noise & material for instance)
- build more compact devices.

Central ITN interest: developing expertise on packaging based on 3D TSV technos.

The applications of 3D vertical interconnects correspond to 3 scales depending the diameter of the vias => the density of vias required by the application.

i) 50-100 μm diameter vias, available on the market (ex connection of services)

ii) 5-10 μm diameter vias, for direct connections between ASICs, or between sensors and the associated processing chips: more and more available in industry

iii) iii) vias ≤1 μm diameter subject to R&D in some high tech firms; requested in very dense systems requiring a pitch between vias of a few μms => e.g. for very advanced digital data processing architecture (massive parallel computing).

INFIERI will investigate some of these applications in collaboration with key industrial firms associated with this project.

WP3: Large Flux Data Transmission

presented by E. Ciaramella & N. Hessey at INFIERI Workshop

WP3 GOALS:

Transfer of data from detector modules to the far-end processors in the cases of CTA, HEP or PET applications thus WP3 address:

- ✧ the specific problems in data transmission for typical length of connectivity ranging from a few tens of cm to about 100 m.
- ✧ transversal-type of activity, which should support the other WP activities.
- ✧ High-rate data transfer, in harsh environments are vital to future experiments => WP3 targets unprecedented transfer rates with low mass, radiation hard devices,
- ✧ novel optical wireless communication, and,
- ✧ given the large number of data links, their interconnectivity.

Electro-optical conversion and coupling to fibre-optics will be developed to integrate to the front-end.

FOM, SSSA and industrial partners (PHILIPS) will go beyond the state-of-the-art GBT chip under development at CERN (5 Gb/s) to reach the rates needed by LHCb (13 Gb/s) and beyond, requiring VDSM & efficient interconnection technologies.

WP3: cont'd

TECHNOLOGIES to be investigated by WP3:

1) **New Si Photonics technologies**, with novel Si multiplexing and light modulators, combining the speed of photonics with the functionality and CMOS fabrication techniques of electronics.

2**) Radio wireless links** with extremely high frequency technology. This relies on VDSM techno, low power 60 GHz transceivers as well as compact low mass directional antennas for 60 GHz.

3) Optimized systems based on **Wavelength Division Multiplexin**g (WDM), able to transmit high speed data fluxes, possibly using advanced modulation formats and detection schemes.

4) **Advanced optical fibre sensor technologies** for distributed and discrete monitoring of various parameters (strains, temperature, humidity, pressure etc.), in harsh environments

5) **Advanced Optical wireless communication** (OWC) system solutions, using either visible or infrared for high data rate transmission, as a viable alternative to RF wireless for reliable and rapid Deployment.

The latency problem is crucial for both HEP and Astrophysics and will be also part of the training and developments of this project.

WP4: Far End Advanced Digital Processing, MPC

presented by Ph Bonnot & F. Lemonnier at INFIERI Workshop

WP4 is essential for CTA, PET and LHC:

- The CTA-HLT will combine & appropriately handled the information from all the individual telescopes of the network.
- Innovative aspect of PET application: include a high level processing to treat the information delivered by this highly pixelated device.
- CMS L1 Trigger will need to match the charged tracks with the calorimeters or the muon systems information to identify peculiar features of the interesting physical processes (similar need for ATLAS) ***Combinatorial challenge: comparing in real time the hits from several layers to pre-calculated tracks at once*** => Use powerful, massively parallel FPGAs and ASICs into Associative Memory chip (AM). The problem is solved in just the time needed to load the data into the AM devices (Pioneered by CDF in SVT)

Aim: improvement by using new FPGAs, which accommodate faster and denser bank patterns, as well GPUs.

WP4: Advanced Digital Processing, MPC cont'd

A longer-term approach: Advanced Massive Parallel Computing

Advanced digital data processing architecture based on Tiers of CAMs (Content Addressed Memories) plus FPGAs; the CAMs are assembled into multi-tier layers interlinked through dense TSV (vias), also used to connect to the controller tier.

These stacks of RAMs/CAMs aim to build a high performance MPC architecture.
The ASICs will use VDSM technology. The high-tech firms that are manufacturing CAM/RAM are using extremely VDSM technos. THALES TRT &SAMSUNG will be closely involved in this part of the project
Similarly the USA associates will bring their complementary skills in this WP4 exploratory study aspect.

Another aspect: the back-end interconnectivity: ATCA framework

When the filtered information from the local data reduction arrives from the FE, it should be routed to the back-end processor (WP4).
Advanced Telecommunications Computing Architecture (ATCA) includes a series of specifications that incorporates the latest trends in high speed interconnect technologies, next generation processors and improved reliability, manageability and serviceability => potentially attractive for our applications.

WP5: Transversal tools

Presented by R. Patti at the INFIERI Workshop

A series of tools that are of use for various work packages will be developed with the corresponding training. These tools include:
i) Kit tools for design and layout of circuits in VDSM CMOS technology,
ii) All types of simulation studies,
iii) Complex pattern recognition software packages,
iv) Lab test bench hardware and software tools (possibly including test beams) for testing specific components or technologies. These different aspects will be achieved with the complementary expertise available within the partners of the proposed network including some industrial partners.

One essential issue we will tackle in this first workshop is: What foundry to choose and thus what why to go for VDSM technology? (R. Patti is expected to give us an overview of the possibilities and we expect inputs from other experts in the consortium)

WP6: System integration studies & test benches

Panel discussion summarizing availabilities in INFIERI consortium

This work package includes:
i) The simulation based study of the system integration related issues in each of the applications,
ii) Design and construction of a mock-up or demonstrator of one or more than one component of the "intelligent data processing chain" and the performances evaluation of this system
iv) Lab test benches or test beams with these prototypes that mimic the real-life functioning of the component, and the analysis of the corresponding performances.

A series of test benches will be developed in the various nodes, and in some cases in the industrial firms, in a coordinated way. They will be adapted to the various demonstrators built by this project
As the prototypes to test are based on novel technologies, developing the corresponding test benches and running them will imply using or building new hardware and software tools.
Another asset of INFIERI is to include world renowned Labs RAL, NIKHEF (full partners) and FNAL and CERN as associate, all with their test facilities and unique expertise.
These test facilities will be a unique training camp for the ESR/ERs and for ensuring this project to achieve its S&T goals.

INFIERI WP's: Deliverables & milestones

WP#	Deliverable No.	Deliverable	Lead Beneficiary *(Contributors)**	Milestones/ Month
1	*1.1*	***Pixel based Level1-Trigger (PT)** feasibility study*	*LIP*	12
	1.2/1.3/1.4	*Prototype design/evaluation & tests results*	*(1,3,4, A3, A4, A10)*	36/48
	1.5	***Outer tracker trigger:** feasibility study*	*INFN*	12
	1.6/1.7/1.8	*Prototype design/ evaluation & tests results*	*(1,A3, A8)*	36/48
	1.9	***CTA-Level1-Trigger** feasibility study*	*UOXF*	12
	1.10/1.11	*Prototype design/ prototype tests results*	(1,4,10, A9, A11)	36/48
	1.12	***PET–Level1-Trigger** feasibility study*	*UC3M*	12
	1.13/1.14	*Prototype design/evaluation & tests results*	*(4,10,A6, A7)*	36/48
2		***VDSM 3D demonstrator + TSV O (10)µm diameter***	CNRS	
	2.1	• *Goals of this study & applications*	(A2, A3, A5, A8)	12
	2.2	• *VHDL design simulation & layout*		*24*
	2.3	• *Tests set-up & results*		*48*
		VDSM 3D studies with TSV O (1)µm diameter	CNRS	
	2.4	• *Study goals & applications*	(A2, A3, A5)	*18*
	2.5	• *Design, simulation, studies with advanced kit*		*48*
3	*3.1*	*High speed link system integration*	FOM (A8, A11)	48
	3.2	*Design of OWC*	SSSA	24
	3.3	*OWC system integration*	SSSA	48
	3.4	*Clock & services/monitoring distribution*	CNRS (A8, A11)	24
	3.5	*Evaluation & report test bench for testing links*	FOM (A8, A11)	48

Deliverables & milestones

4		***CTA-High Level Processing***	ULIV	
	4.1	*VHDL design + algorithm simulation study*	(1,4,10,11,A9,	18
	4.2/4.3/ 4.4	*FPGA based proto/test bench develop tests results*	A11)	36/36/48
	4.5/4.6	***PET-High Level Processing***	INFN	18/36
	4.7/4.8	*VHDL design & algorithms development.*	(2,5,10,11,A6,	36/48
		FPGA-proto/Test bench devpt & proto tests	A7)	
	4.9	*results*		18
	4.10	***HEP- High Level Processing***	STFC	36
	4.11	• *VHDL design and simulation*	(2,3,4,8,A3,A4,	36
		• *Prototype design & construction*	A8, A10)	
	4.12	• *Test bench development & tests results*	TRT	24/48
		Advanced digital processing architectures:	(1, A1, A2, A3,	
		VHDL design and feasibility studies	A8)	
		Tools & characterization test bench for	ALL	
	5.1/5.2/5.3/5.4	• *WP1 /WP2/ WP3 and WP4*	& Associates	48**
5	*5.5*	• *Advanced pattern recognition algorithms*		48**
	5.6	• *Simulation & performance studies*		48**
6		***Integration simulation studies:***	ALL	
	6.1/ 6.2/ 6.3	*Astrophysics/HEP/Medical*	& Associates	48**
		Integration test benches for:	ALL	
	6.4/6.5/6.6	*Astrophysics/ HEP/ Medical*	& Associates	48**

** In parenthesis, for all detailed list, the full partners that will be contributing tit the specific task/deliverable. The associated partners' contributions are indicated as well with the numbering preceded by the letter A.*
*48** is applied for items with a first version ready much before the end of the ITN and with continuous upgrade or. This is the case for instance for the dedicated test benches or the development of simulation packages.*

WP7 and WP8

- TRAINING WP7 and related deliverables will be presented in details in the Workshop. This is a very demanding and also the main topic to which the E.U. financial support is allocated.

- OUTREACH WP8 and related deliverables will be presented in details in the Workshop

=> the INFIERI Workshop presentations/discussions